Four-Element Phased-Array Beamformers and A Self-Interference Canceling Full-Duplex Transceiver in 130-nm SiGe for 5G Applications at 26 GHz

by

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Abstract

This thesis is on the design of radio-frequency (RF) integrated front-end circuits for next generation 5G communication systems. The demand for higher data rates and lower latency in 5G networks can only be met using several new technologies including, but not limited to, mm-waves, massive-MIMO, and full-duplex. Use of mm-waves provides more bandwidth that is necessary for high data rates at the cost of increased attenuation in air. Massive-MIMO arrays are required to compensate for this increased path loss by providing beam steering and array gain. Furthermore, full duplex operation is desirable for improved spectrum efficiency and reduced latency. The difficulty of full duplex operation is the self-interference (SI) between transmit (TX) and receive (RX) paths. Conventional methods to suppress this interference utilize either bulky circulators, isolators, couplers or two separate antennas. These methods are not suitable for fully-integrated full-duplex massive-MIMO arrays.

This thesis presents circuit and system level solutions to the issues summarized above, in the form of SiGe integrated circuits for 5G applications at 26 GHz.

First, a full-duplex RF front-end architecture is proposed that is scalable to massive-MIMO arrays. It is based on blind, RF self-interference cancellation that is applicable to single/shared antenna front-ends. A high resolution RF vector modulator is developed, which is the key building block that empowers the full-duplex front-end architecture by achieving better than state-of-the-art 10-b monotonic phase control. This vector modulator is combined with linear-in-dB variable gain amplifiers and attenuators to realize a precision self-interference cancellation circuitry. Further, adaptive control of this SI canceler is made possible by including an on-chip low-power IQ downconverter. It correlates copies of transmitted and received signals and provides baseband/dc outputs that can be used to adaptively control the SI canceler. The solution comes at the cost of minimal additional circuitry, yet significantly eases linearity requirements of critical receiver blocks at RF/IF such as mixers and ADCs.

Second, to complement the proposed full-duplex front-end architecture and to provide a more complete solution, high-performance beamformer ICs with 5-/6-b phase and 3-/4-b amplitude control capabilities are designed. Single-channel, separate transmitter and receiver beamformers are implemented targeting massive-MIMO mode of operation, and their four-channel versions are developed for phased-array communication systems. Better than state-of-the-art noise performance is obtained in the RX beamformer channel, with a full-channel noise figure of 3.3 dB.

26 GHz 5G Uygulamaları için 130-nm SiGe Teknolojisiyle Dört-Kanallı Faz-Dizili Hüzmeleyici ve Özgirişim Kaldıran Tam Dubleks Alıcı/Verici Geliştirilmesi

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Özet

Bu tez, yeni nesil 5G iletişim sistemleri için radyo frekansı (RF) entegre ön uç devrelerinin tasarımı üzerinedir. 5G şebekelerinde yüksek veri oranları ve düşük gecikme süreleri ancak milimetrik dalgalar, masif-MIMO ve tam dubleks vb. gibi bir kaç yeni teknolojinin beraber kullanılması ile karşılanabilir. Milimetrik dalgaların kullanılması, havadaki zayıflama kayıplarını artırsa da, yüksek veri hızları için gerekli olan daha fazla bant genişliğini sağlar. Artan yol kayıplarını telafi etmek için masif-MIMO dizileri, hüzme şekillendirmek ve dizi kazancı sağlamak için kullanılır. Ayrıca, yüksek spekturum verimliliği ve düşük gecikme süresi için tam dubleks sistemler istenmektedir. Tam dubleks sistemlerin güçlüğü ise iletim (TX) ve alıcı (RX) arasındaki öz girişimdir (SI). Sirkülatörler, izolatörler, kuplörler veya iki ayrı anten kullanımı bu etkileşimi bastırmak için kullanılan geleneksel yöntemlerdir. Ancak bu yöntemler tam-entegre tam dubleks masif-MIMO dizileri için uygun değillerdir.

Bu tez, 26GHz'de 5G uygulamaları için yukarıda özetlenen sorunlar hakkında SiGe teknolojisiyle devre ve sistem düzeyinde çözümler sunmaktadır.

İlk olarak, masif-MIMO dizileri için ölçeklenebilir bir tam-dubleks RF ön uç mimarisi önerilmiştir. Tekli/paylaşımlı anten sistemleri özelinde, dışarıdan girdi almaksızın RF özgirişim baskılamak üzerinedir. Bu amaçla, tam dubleks ön uç mimarisini gerçeklemede kritik rolü olan yüksek çözünürlüklü bir RF vektör modülatörü geliştirilmiştir. Bu modulatör literatüden daha iyi olarak, 10-bit monotonik faz kontrolü sağlamaıştır. Bu vektör modülatörü, hassas bir öz girişim engelleme devresi gerçekleştirmek için dB-lineer değişken kazançlı yükselteçler ve zayıflatıcılarla birleştirilmiştir. Dahası, özgirişim baskılayıcının uyarlanabilir kontrolü için, bir kırmık üstü düşük güçlü IQ aşağı dönüştürücüsü entegre devreye dahil edilmiştir. Bu yapı, iletilen ve alınan sinyallerin kopyalarını korele eder ve uyarlamalı kontrol için kullanılabilecek temel bant/dc çıkışları sağlar. Çözüm, asgari ek devre maliyetine sahip olmakla birlikte, karıştırıcılar ve ADC'ler gibi RF/IF'deki kritik alıcı blokların doğrusallık gereksinimlerini önemli ölçüde kolaylaştırmaktadır.

İkinci olarak, önerilen tam-dubleks ön uç mimarisini tamamlamak ve daha eksiksiz bir çözüm sağlamak için, 5-/6-b faz ve 3-/4-b genlik kontrol yetenekleri olan yüksek performanslı hüzme şekillendirici entegre devreleri tasarlanmıştır. Tek kanallı alıcı ve verici devreleri masif-MIMO uygulamaları için, dört kanallı alıcı ve verici devreleri ise faz dizinli hüzme şekillendirme uygulamaları için geliştirilmiştir. Tekli alıcı kanalında, literatürdeki tüm örneklerden daha iyi olarak, 3.3 dB'lik gürültü seviyesi elde edilmiştir.

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List of Abbreviations

AF	Array Factor
AM	Amplitude Modulation
ATT	Attenuator
BPSK	Binary Phase Shift Keying
CB	Common-Base
CE	Common-Emitter
COTS	Custom Off-The-Shelf
CPWG	Co-Planar Waveguide with lower Ground plane
DBF	Digital Beam Forming
EBD	Electrical Balance Duplexer
EIRP	Equivalent Isotropically Radiated Power
FD	Full Duplex
FDD	Frequency Division Duplex
FM	Frequency Modulation
$\mathbf{f_{Max}}$	Maximum Oscillation Frequency
FOM	Figure-of-Merit
$\mathbf{f_T}$	Maximum Transit Frequency
GaAs	Gallium-Arsenide
HD	Half-Duplex
HP	High Pass
IBFD	In-Band Full-Duplex
IC	Integrated Circuit
IF	Intermediate Frequency
IHP	Innovations for High-Performance Microelectronics
$\mathbf{IIP_3}$	Input-Referred Third-Order Intercept Point
IL	Insertion Loss
IMD	Intermodulation Distortion
InP	Indium phosphide
iNMOS	Isolated NMOS
IP1dB	Input 1-dB Compression Point
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Low Pass
LTE	Long-Term Evolution
MIM	Metal-Insulator-Metal
MIMO	Multiple-Input Multiple-Output
MMIC	Monolithic Microwave Integrated Circuits
mm-Wave	Millimeter-wave
MOS	Metal-Oxide-Semiconductor
NF	Noise Figure
$\mathbf{OIP_3}$	Output-Referred Third-Order Intercept Point
$\mathbf{OP_{1dB}}$	Output 1-dB Compression Point
PA	Power Amplifier
PAE	Power-Added-Efficiency
PS	Phase Shifter
QAM	Quadrature Amplitude Modulation

RADAR	Radio Detecting And Ranging
RF	Radio Frequency
RMS	Root Mean Square
RTPS	Reflection Type Phase Shifter
RX	Receiver
SAW	Surface Acoustic Wave
SI	Self-Interference
SiGe	Silicon-Germanium
SNR	Signal-to-Noise Ratio
SPDT	Single-Pole Double-Throw
T/R	Transmit/Receive
TDD	Time Division Duplex
TX	Transmitter
VGA	Variable Gain Amplifier

Chapter 1

Introduction

1.1 A Brief History of Mobile Wireless Communications

The concept of cellular communications is based on using a large number of base stations, each serving the end users within a specified area or cell. For the mobile terminal, the base station provides access to the cellular network, which is deployed via fiber optic cables or point-to-point links. This concept revolutionized mobile communications by significantly lowering the cost as it enabled the reuse of frequency resources simultaneously in different base stations.

Starting from 1980, a new generation of mobile communication systems has been deployed for almost every 10 years [1]. The first generation (1G) systems used analog modulation techniques, circuit switching, and frequency division multiple access (FDMA). The increasing demand for more capacity per cell led the development of 2G (GSM) technologies that relied on digital communication systems, time-division multiple-access (TDMA) with frequency-division duplexing (FDD), but still using circuit switched networks. The demand for high-speed internet connections and live video communications were the main driving force behind 3G systems (UMTS, IMT2000). They were based on wideband code-division multiple access (WCDMA) and packet switching technology, therefore providing broadband data service [2]. 4G/LTE, which is a completely IP based technology, achieved even higher data

Table 1.1: History of 1G, 2G, 3G, and 4G standards [3].

	Various generations				
Technology	**1G**	**2G**	**2.5G**	**3G**	**4G**
Design began	1970	1980	1985	1990	2000
Implementation	1984	1991	1999	2002	2012–2015
Service	Analogue voice	Digital voice	High-capacity packets, MMS	High-capacity broadband data	Higher capacity, completely IP, Multimedia
Multiple access	FDMA	TDMA, CDMA	TDMA, CDMA	CDMA	OFDMA
Standards	AMPS, TACS, NMT	CDMA, GSM, PDC	GPRS, EDGE	WCDMA, CDMA2000	Single standard
Bandwidth	1.9 kbps	14.4 kbps	384 kbps	2 Mbps	200 Mbps
Core network	PSTN	PSTN	PSTN, Packet network	Packet network	Internet

rates with orthogonal frequency division multiple access and using internet as its core network. It is fascinating to see that today's LTE-Advanced systems almost achieve Shanon capacity at the link level. Yet, there are rapidly growing expectations for 5G as we approach 2020.

1.2 What is 5G?

There is a growing demand of mobile users for improved broadband performance, to enable technologies such as ultra HD video streaming and cloud services. There are also upcoming application areas such as internet-of-things (IOT), machine-to-machine communications, wearable consumer electronics, smart homes/cities, autonomous cars/drones and remote medical services. These are challenging applications to realize with current wireless communication technologies. To meet these demands, next generation (5G) mobile communication systems target higher data rates and capacity, lower latency, better link robustness and energy efficiency.

International Telecommunication Union (ITU) has set challenging specifications to answer these demands, as seen in Fig. 1.1: Peak data rates up to 10 Gb/s with a minimum cell edge data rate of 100 Mb/s, close to 10 bits/s/Hz spectral efficiency, mobility up to 500 km/h, cost efficiency at least 10x better than 4G, around 1 M simultaneous connections per km^2 and latency less than 1 ms [4]. Currently, there is

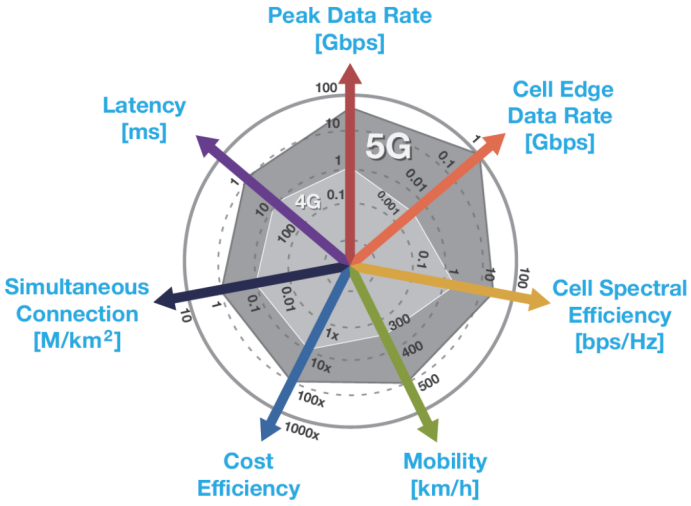


Figure 1.1: Expected 5G performance requirements [4].

not a consensus on what 5G will look like to deliver such high level of performance. ITU plans for 5G standardization to take place within IMT-2020 specifications. However, the necessity for new technologies such as mm-waves, small cells, massive MIMO, beamforming and full duplex are widely agreed upon [4–8].

Higher data rates can be achieved using *mm-waves* (30-300 GHz) that offers more bandwidth. However, mm-waves suffer from increased propagation losses in air. In addition, mm-wave propagation is highly affected by rain, blockage and reflections. Therefore, mm-waves necessitate the use of *small cells* [5]. These are miniaturized base stations that will be densely deployed throughout the cities, operating at lower power levels compared to standard base stations. To increase the channel capacity, these small cells will employ *massive MIMO* (multiple-input multiple-output) structures, i.e. hundreds of antennas in an array. This enables providing service to many more users at the same time. In addition, these arrays can be used for *beamforming*, which also compensates for the increased path loss of mm-waves by providing an array gain factor towards a specific user. Finally, to further improve the spectral efficiency and reduce the network latency, *full-duplex* radio operation is expected as part of 5G networks, that is simultaneous radio transmission and reception.

Full duplex operation requires very high isolation between transmit (TX) and receive (RX) ports. If TX and RX uses the same antenna, isolation may be obtained using either a circulator, hybrid or directional coupler. Alternatively, TX and RX

can use two separate antennas. The former methods reduce TX output power and degrades RX noise figure, whereas the latter method consumes 2× more antenna area. Furthermore, if two separate antennas are used for TX and RX, it is not possible to construct a single array. In that case, two separate antenna arrays, one for TX and one for RX is required.

It is expected that 5G technology will utilize sub-6 GHz bands as well as licensed bands at 26/28 GHz [9]. It has been argued that massive-MIMO systems with fully digital and distributed array architectures will dominate 5G applications at sub-6 GHz bands. However, at mm-wave frequencies hybrid beamforming architectures are proposed. As mm-wave antennas are inherently small, some portion of a large array can be combined to form analog subarrays to be used for a single user.

Therefore, small cell base stations with mm-wave massive-MIMO or phased-array transceivers are a promising candidates for 5G networks. However, using the same antenna for both TX and RX is currently not feasible without bulky off-chip blocks mentioned above. So, currently full duplex operation is not compatible with mm-wave beamforming systems.

1.3 Thesis Overview

This thesis is on the design of radio-frequency (RF) integrated front-end circuits for next generation 5G communication systems. The demand for higher data rates and lower latency in 5G networks can only be met using several new technologies including, but not limited to, mm-waves, massive-MIMO, and full-duplex. Use of mm-waves provides more bandwidth that is necessary for high data rates at the cost of increased attenuation in air. Massive-MIMO arrays are required to compensate for this increased path loss by providing beam steering and array gain. Furthermore, full duplex operation is desirable for improved spectrum efficiency and reduced latency. The difficulty of full duplex operation is the self-interference (SI) between transmit (TX) and receive (RX) paths. Conventional methods to suppress this interference utilize either bulky circulators, isolators, couplers or two separate antennas. These methods are not suitable for fully-integrated full-duplex massive-MIMO arrays.

This thesis presents circuit and system level solutions to the issues summarized above, in the form of SiGe integrated circuits for 5G applications at 26 GHz.

First, a full-duplex RF front-end architecture is proposed that is scalable to massive-MIMO arrays. It is based on blind, RF self-interference cancellation that is applicable to single/shared antenna front-ends. A high resolution RF vector modulator is developed, which is the key building block that empowers the full-duplex front-end architecture by achieving better than state-of-the-art 10-b monotonic phase control. This vector modulator is combined with linear-in-dB variable gain amplifiers and attenuators to realize a precision self-interference cancellation circuitry. Further, adaptive control of this SI canceler is made possible by including an on-chip low-power IQ downconverter. It correlates copies of transmitted and received signals and provides baseband/dc outputs that can be used to adaptively control the SI canceler. The solution comes at the cost of minimal additional circuitry, yet significantly eases linearity requirements of critical receiver blocks at RF/IF such as mixers and ADCs.

Second, to complement the proposed full-duplex front-end architecture and to provide a more complete solution, high-performance beamformer ICs with 5-/6-b phase and 3-/4-b amplitude control capabilities are designed. Single-channel, separate transmitter and receiver beamformers are implemented targeting massive-MIMO mode of operation, and their four-channel versions are developed for phased-array communication systems. Better than state-of-the-art noise performance is obtained in the RX beamformer channel, with a full-channel noise figure of 3.3 dB.

1.4 Thesis Organization

The next chapter provides the fundamentals of first phased array systems and then full-duplex communications. The chapter follows by presenting the current state-of-the-art in both fields.

Chapter 3 covers the analysis, design, and measurements of the full-duplex transceiver that employs an on-chip accurate SI canceler circuitry, together with a low-power IQ downconverter for monitoring and self-adaptability purposes. The

chapter starts with the system level analysis of the key design criteria such as amplitude/phase control resolution and RX linearity, continues with a presentation of the realized I/Q vector modulator achieving monotonic 10-b phase resolution and its implementation details, and concludes by providing the details of the rest of the building blocks and the operation of the overall full-duplex transceiver.

Chapter 4 contains the work related to beamforming ICs for massive-MIMO and phased-array applications. The chapter begins with the implementation details of the single RX channel and its sub-blocks, presenting the novel design methodologies of the amplitude/phase control blocks. The chapter continues with extensive measurement results regarding the RX and TX channels. Finally, the chapter concludes by presenting the development of four-element TX and RX beamforming ICs, the required modifications performed for each subblock, the flip-chip packaging considerations, and most recent simulation results.

Finally, Chapter 5 summarizes the main findings and contributions of this dissertation as well the impact of the results, provides a list of future work to do, discusses the limitations of the proposed ideas and offers possible solutions, and finally suggests a possible way of combining the full-duplex and beamforming ICs developed in this dissertation.

Chapter 2

Background

2.1 Phased Arrays

2.1.1 Operating Principles

A single antenna element exhibits a relatively low directivity, meaning that the radiation is in all directions (omnidirectional), i.e. it has a very wide main beam. If a number of antennas are deployed in an array formation, the overall antenna becomes much more directive, i.e. the main beam gets narrower. If the phase of each radiating element is controlled properly (i.e. with a constant phase taper between each adjacent elements), this main beam can be steered away from the normal direction. In addition, if the amplitude of each radiating element is control properly (i.e. by applying a weighting window), the position of beam side lobes as well as beam null positions can be controlled.

Fig. 2.1 shows a system level phased array receiver [10]. Assume there is a phase shifter in each channel, providing a phase taper of $\Delta\phi$ between adjacent channels. If this phase taper is chosen as $\Delta\phi = 2\pi\frac{d\sin\theta}{\lambda}$, the main beam direction of the array is steered θ degrees away from the antenna normal. That is because, the signals coming from this angle are combined constructively, while the signals coming from other directions are combined de-constructively. The same operation also holds if the array is used as a transmitter rather than a receiver. Therefore, a phased array performs spatial filtering and combining in receive and transmit modes, respectively.

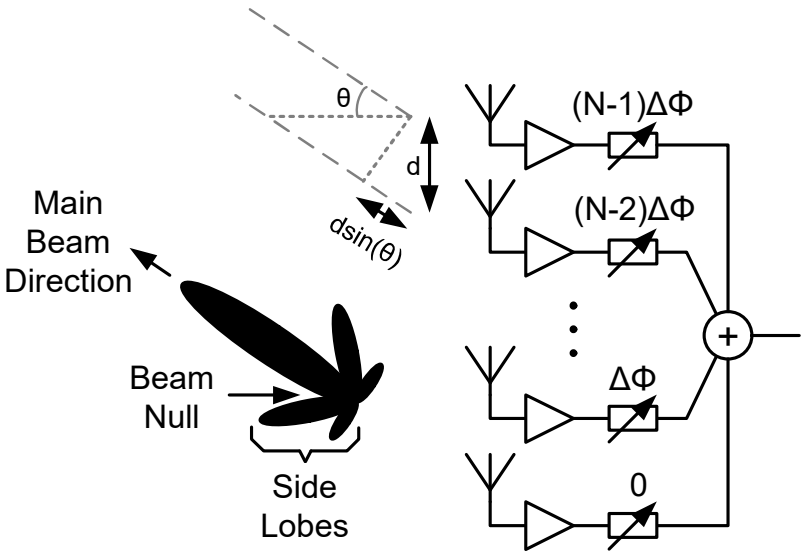


Figure 2.1: A phased array receiver with N elements [10].

The above mentioned phased array operation has been well known and utilized since 1940-50s, especially in the form of military RADARs [11, 12]. In recent years, with the advancements in integrated circuit technologies antenna arrays are started to appear in commercial applications as well, such as wireless LAN, cellular communications and autonomous vehicles. In communication systems where the number of users is much smaller than the number of antenna elements, the system is called massive MIMO [9]. In these systems, different beams are generated for each user simultaneously. Due to the large number of antennas, these beams can be made orthogonal to each other, i.e. all users can be served using the same time/frequency resource.

2.1.2 Phased Array Architectures

Instead of the constant phase taper shown in Fig. 2.1, a more complicated control can be applied as well. This process of generating a desired beam shape is called beamforming. Beamforming can take place either in analog or digital domains. Analog beamforming (Fig. 2.2.a) is often implemented using RF phase shifters. Most of the time these are digitally controlled phase shifters, providing 4-6 bit phase resolution. Their performance is limited by phase quantization that makes it difficult to fine tune the beam shape. On the other hand, analog phase

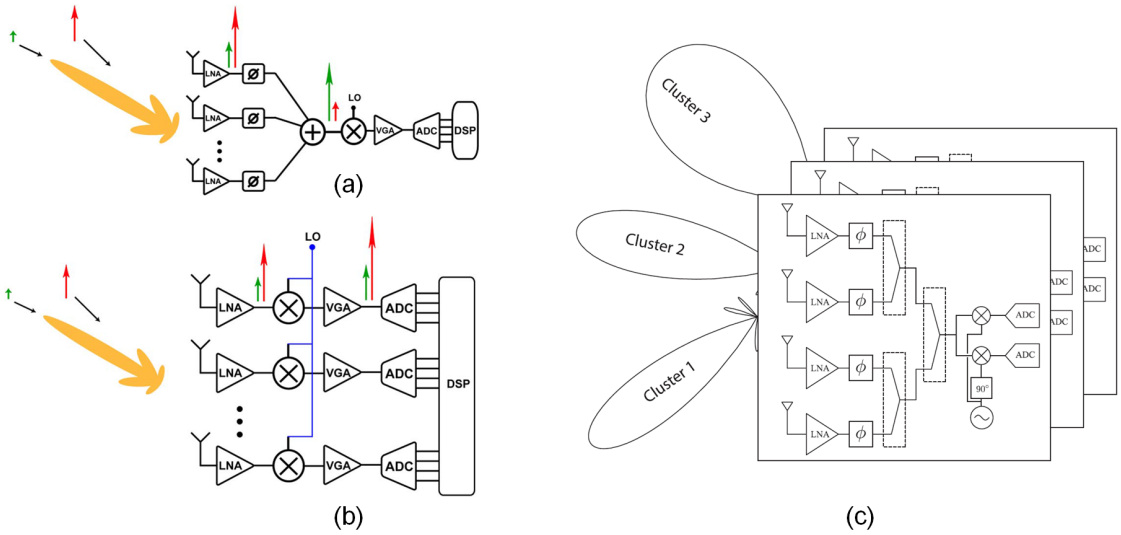


Figure 2.2: Different beamforming architectures: (a) analog, (b) digital, and (c) hybrid [9].

shifters require high-resolution DACs, hence digitally controlled phase shifters are still preferred.

In analog beamforming, signals coming from different antennas are combined prior to analog-to-digital conversion. So, the desired signal (main beam) is enhanced and undesired interferers are suppressed before the ADC. However in digital beamforming (Fig. 2.2.b), signals coming from each antenna is first digitized and signal combining takes place in the digital domain. This poses very high linearity requirements for ADCs. Furthermore, digital beamforming can support any number users, only limited by the number of antennas in the array. On the other hand, if analog beamforming is used, a separate analog beamformer is required for each user.

A popular approach for 5G is the so-called hybrid-beamforming (Fig. 2.2.c), which is a trade-off between analog and digital beamformers [13]. In this approach, a large array of N_A antennas are driven by N_R distinct analog/RF beamformers that are controlled by digital beamformers supporting N_U number of users. As long as $N_A > N_R > N_U$ is satisfied, this system acts as a multi-user MIMO.

Phased arrays are especially useful at mm-wave frequencies. Why? Because, even if the atmospheric attenuation increases at mm-wave frequencies, the antenna sizes get smaller. So, for the same aperture size, one can use an antenna array, obtaining a much larger antenna directivity and gain compared to RF frequencies.

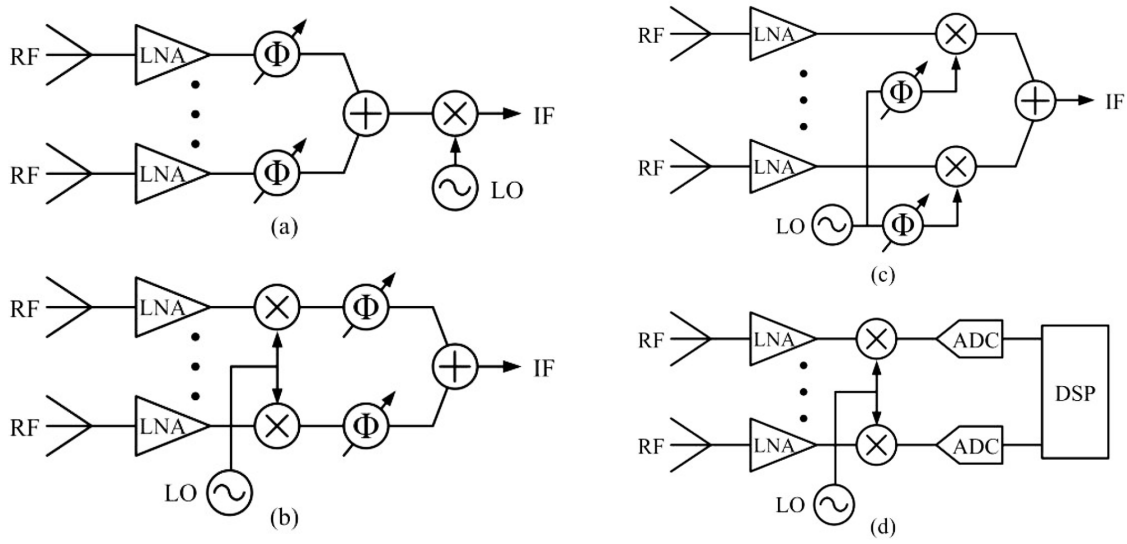


Figure 2.3: Different phase shifting methods: (a) RF, (b) IF, (c) LO and (d) digital.

The ability to steer the beam and the ability to reject interferers by spatial filtering are the added benefits.

Many works can be found in the literature on Silicon-based phased arrays operating at 60 GHz and beyond, for various applications such as high data rate short range communications [14–16], automotive radar [17], and mm-wave backhaul [18]. Wafer-scale phased-arrays have been demonstrated including as many as 256 elements using reticle-stitching [19]. Phased array transceivers with polarization diversity [14] and concurrent dual polarization [20, 21] have been developed.

2.1.3 Phase Shifting Methods

In phased array architectures, the phase shift can be obtained by various means, which can be grouped into four major categories: RF phase shifting, LO phase shifting, IF phase shifting and digital phase shifting, as can be seen in Fig. 2.3.

RF phase shifting is the most popular and succesful option among the four possibilities for several reasons. First, it employs a single mixer, avoiding the complex LO distribution networks. Second, in RF phase shifting, constructive/deconstructive interference of signals coming from different antennas take palce *befor* the mixer. This way the mixer linearity requirement is relaxed immensely, since the interferers will be subject to spatial rejection of the RF beamformer.

2.1.4 Existing Literature in 26/28 GHz Integrated Phased Array Transceivers for 5G

A significant amount of research has been conducted on 5G mm-Wave transceivers for the 26/28 GHz bands, both by academia and industry. For instance, Kodak [22–24] presented a number of bidirectional phased-array channels in 45-nm CMOS SOI, achieving as low as 3.7 dB NF and supporting up to 64-QAM/500-MBaud modulation bandwidths, using switched-LC phase shifters. The same phase shifting topology was also utilized in [25] to realize a dual-polarization phased-array transceiver with 24-channels in bulk-CMOS, and also in [26] to realize a direct conversion phased array transceiver.

IQ vector modulator based phase shifters were reported as well [27–31], in which scalable 32- and 64-element phased-array transceivers are realized, and 8-12 Gbps 5G communication links were demonstrated at 300 meters. Using polarization diversity, 24 Gbps 64-QAM 2×2 MIMO link has been recently reported [31].

Alternative RF phase shifting methods were also investigated. For instance, a tunable tranamission line was utilized in [32] to implement a 32-element TRX phased-array with dual-polarization and orthogonal phase/gain control. Further, low power phased array receiver front-ends have been reported utilizing RTPSs [33].

Although not as common as RF phase shifting, LO phase shifting and digital beamforming techniques can also be seen in the literature. For example, Pang [34] presented a 28 GHz CMOS phased-array transceiver featuring gain invariance based on LO phase shifting architecture with 0.1-degree beam-steering resolution for 5G new radio. Yang demonstrated a 28 GHz 64-channel MIMO transceiver with a fully digital beamforming architecture [35].

Recently, there has been a growing demand on hybrid beamforming architectures. One such exmaple is [36], which presented 25-30 GHz fully-connected hybrid beamforming receivers for MIMO communication. He also presented [37] 28/37 GHz hybrid beamforming MIMO receiver with carrier aggregation and RF-domain LMS weight adaptation.

Unconventional forms of beamforming, such as dual-vector distributed beam-

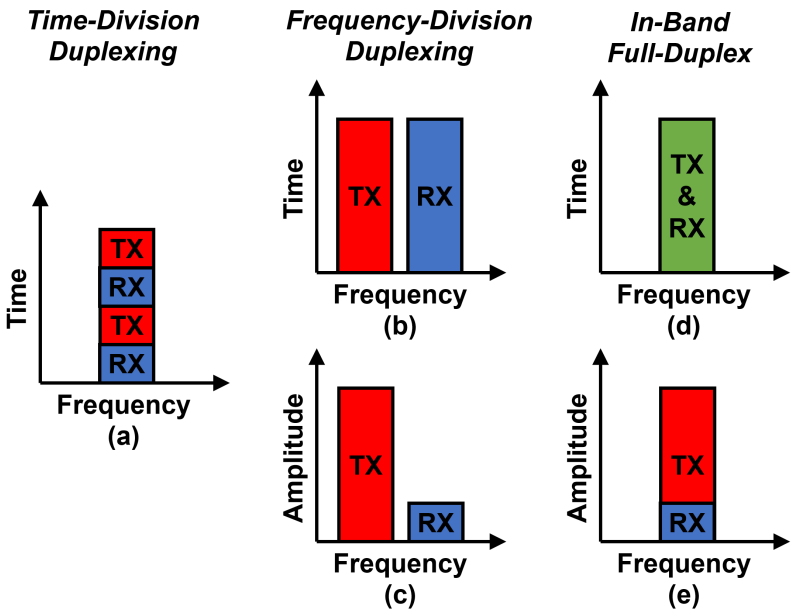


Figure 2.4: Conceptual copmarison of TDD, FDD, and IBFD operation.

forming [38,39] and self-steering beamforming [40,41] have also been reported in the literature.

2.2 Full Duplex Radio

2.2.1 Operating Principles

In addition to massive-MIMO and/or phased-array beamforming full-duplex operating radios are proposed as an enabler for future 5G networks [1]. By full duplex, in this dissertation, we refer to in-band full duplex (IBFD), i.e. a terminal transmitting and receiving at the same frequency. Fig. 2.4 shows conceptually the difference between TDD, FDD, and IBFD mode of operation. In theory, IBFD doubles the spectral efficiency (bits/s/Hz) compared to the other to duplexing schemes. Additionally, full-duplex solves problems other than physical layer, such as collision detection and hidden terminal.

The reason full duplex is not widely used today is the self-interference problem, that is the coupling from a transmitter to its own receiver. Typically, more than 100 dB self interference suppression is required for a full duplex link to achieve an SNR equal to its half duplex counterpart [42]. Even though the transmitted

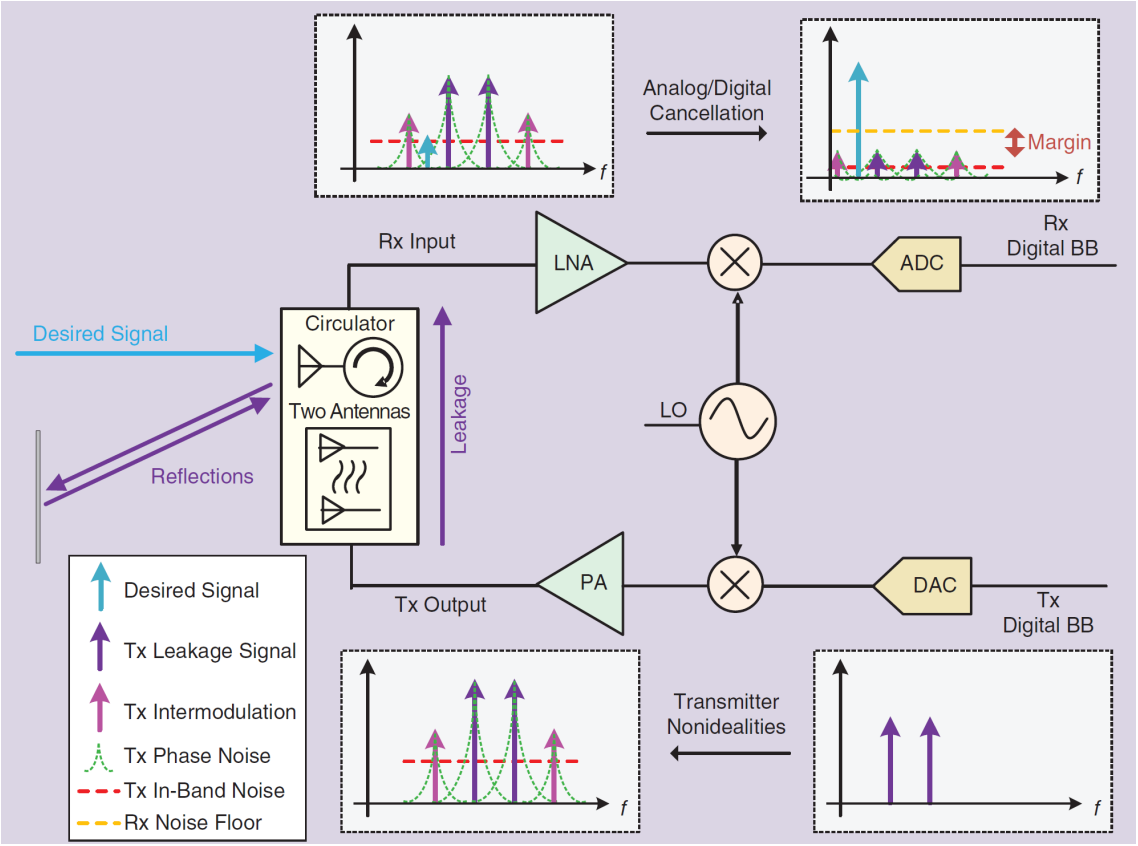


Figure 2.5: Generic full-duplex transceiver architecture depicting the main self-interference signal, its multiple reflections from the environment, and TX nonidealities, all of which must be suppressed below the noise floor to achieve sufficient SNR for the desired signal [42].

signal is known, this amount of self-interference cancellation cannot be performed in digital domain, mainly due to limited ADC dynamic range, but also due to oscillator phase noise, mixer and amplifier nonlinearities and I/Q mismatches. So, additional suppression and cancellation is required in antenna and analog domains prior to ADCs. Some of these techniques are antenna separation, cross-polarization and active analog cancellation, i.e. tapping a copy of the transmitting signal and subtracting it from the received signal after adjusting its amplitude and phase/delay. Although these and many more full duplex techniques are well known and have been tried for ages, the reason why full duplex is currently a hot research topic is that other methods of increasing spectral efficiency (advanced modulations, coding, MIMO) have been exhausted. Another motivation is the trend towards smaller cells that makes the self-interference problem more manageable [43].

Assume a full duplex WiFi radio with a 80 MHz bandwidth, 20 dBm transmit

power and 5 dB receiver noise figure. The noise floor of this particular receiver becomes $-174 + 10\log(80 \times 10^6) + 5 = -90$ dBm. In this scenario we need 110 dB overall self-interference suppression/cancellation distributed across antenna/propagation, analog/RF and digital domains in order to push self-interference below the noise floor. Assuming a 50 dB digital cancellation, which is feasible using a typical 12-bit (~70 dB dynamic range) ADC, 60 dB RF and antenna cancellation is required.

2.2.2 Duplexers/Circulators

Traditionally, duplexing has been performed using separate antennas for RX and TX. When a single antenna is shared for both RX and TX, duplexing is achieved using polarization diversity or with circulators. In [44] a two antenna with cross-polarized RX and TX operation is proposed. Further suppression of the SI signal is achieved by tunable reflection termination of an auxiliary port introduced to the RX antenna that is copolarized with the TX antenna. The technique is applicable to both RF and mm-wave frequencies. However, the technique is not applicapble to massive-MIMO and phased-array architectures due to the use seperate RX and TX antennas.

An alternative way of duplexing using the electrical balance of a hybrid transformer was introduced in [45, 46], although for FDD systems. It relies on electrical balance rather than frequency selectivity, making it possible to integrate with CMOS RFICs, as it does not require high-Q passive components. During the last decade it has been widely used and studied at RF frequencies. A fully-differential version was developed [47] and combined with an antenna impedance tracking loop [48]. Its bandwidth limitation has been studied and 62 dB isolation was achieved across 20 MHz bandwidth [49]. A dual-notch version was developed that achieves $>$ 40 dB isolation across 160 MHz bandwidth [50]. An even superior performance (+70 dBm IIP_3) was later obtained thanks to the development of SOI CMOS processes [51]. A different version was developed using a floating balancing network to achieve low noise operation [52]. Combining EBDs with SAW filters [53], and later on

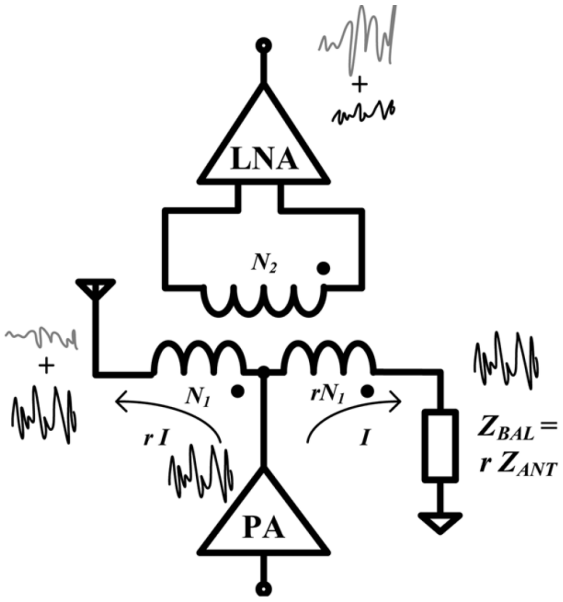


Figure 2.6: Hybrid-transformer based electrical-balance duplexer [48].

with N-path filters [54] resulted in tunable front-ends supporting both FDD and IBFD modes of operation. Today, EBDs provide state-of-the-art performance at full-duplex RF (< 3 GHz) systems [55].

Despite all these demonstrations, EBD performance at mm-wave frequencies is still sub-par. First, the effect of coil parasitics, both the shunt capacitance to the substrate and the inter-winding capacitance, limits the achievable isolation and increases insertion loss.

In addition to antenna pair and electrical balance duplexers, recently nonmagnetic circulators have been developed in integrated circuits, to replace ferrite circulators that are bulky and impossible to integrate with silicon [56–59]. They are forms of linear periodically time-varying circuits, utilizing either N-path filters (for RF) or periodically switched transmission lines (for mm-wave), which is also called spatio-temporal conductivity modulation, to achieve nonreciprocity. Although initial findings are promising, further research is necessary to fully appreciate the concepts that try to break the Lorentz reciprocity.

2.2.3 SI Cancellation Techniques

It might seem easy for a transceiver to cancel out its own transmitted signal since the transmitted signal is known in advance, however this is not the case for several

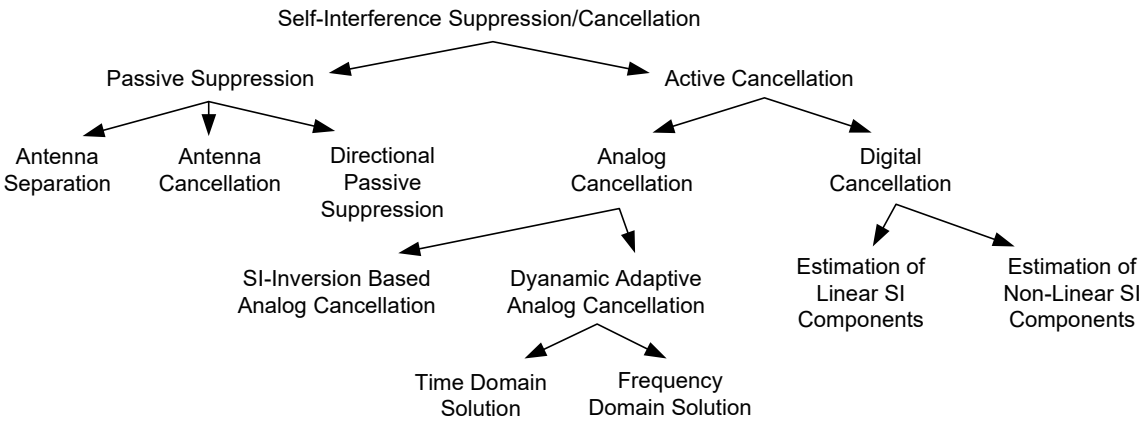


Figure 2.7: List of self-interference cancellation and suppression techniques [62].

reasons: First, TX to RX leakage signal experiences small but not negligible delay. Second, the transmitted RF signal is a distorted copy of the transmitted baseband signal mainly due to PA nonlinearity and LO phase noise (For a detailed analysis regarding the impact of phase noise on digital self-interference cancellation in full-duplex systems, the reader may refer to [60].). Third, the signal at the receiver also include multiple reflections from the nearby environment in addition to the main leakage from TX to RX via the antenna or circulator [61].

A collection of techniques related to self-interference cancellation can be seen in Fig. 2.7. In antenna separation approach, TX and RX antennas are physically separated and isolation is obtained from path loss between antennas. In antenna cancellation method, two transmit antennas are placed d and $d + \lambda/2$ away from the receiver antenna so that they interfere destructively. In directional passive suppression, TX and RX antennas (or arrays) are positioned such that their main lobes have minimal interaction. The first and third methods require two separate antenna arrays, while the second method does not allow even a single array for TX or RX. So, these methods are not suitable to massive-MIMO and phased-array systems [62].

Active SI cancellation techniques will be covered in the following sections.

2.2.4 Adaptive SI Cancellation

In practice it is desirable to have a self-adaptive scheme to achieve the required SI cancellation performance. The literature on self-adaptive techniques and adaptive filters is vast. Here discussion will be limited to their use in full-duplex radios, with

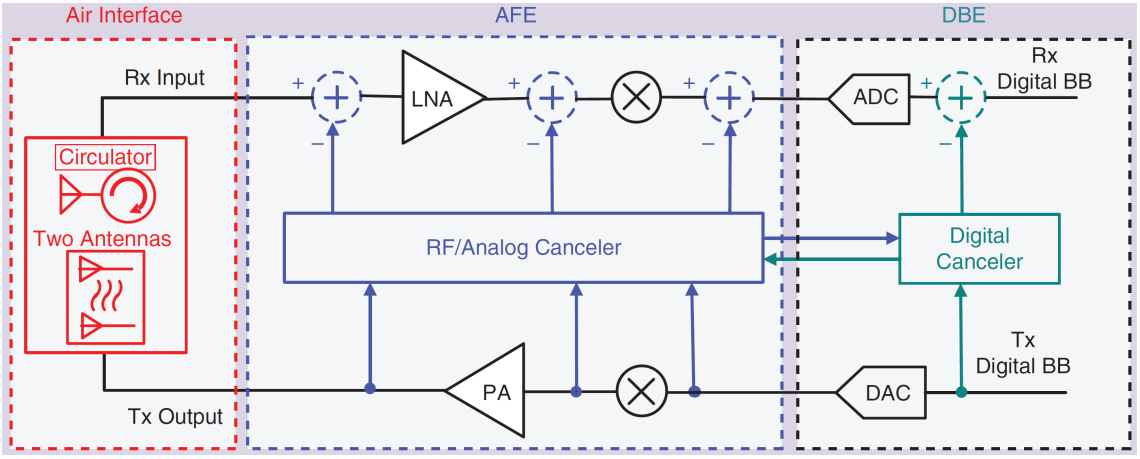


Figure 2.8: Self-interference suppression/cancellation techniques in different domains: antenna/propagation domain, analog/RF domain, and digital domain [42].

an emphasis on hardware/IC implementations.

Adaptive filters date back to 60s and they utilize some form of the least-mean-squares (LMS) algorithm, which is shown in Fig. 2.9. These are best applicable to digital filters. However, analog/RF SI cancellation is necessary for FD communications to achieve a reasonable signal-to-interference ratio before converting the signal to digital domain, as the dynamic range of high-speed ADCs are limited. Therefore, hardware/RF implementations of the LMS adaptive filter has also been reported in the literature. For example, Aparin implemented an integrated LMS adaptive filter of TX leakage for CDMA receiver front ends [63]. Although it is not a FD system, the results and conclusions are applicable to FD systems. They utilize analog multipliers to correlate the LNA output signal with quadrature copies of the transmitted signal. This is a direct implementation of the 2-tap digital LMS filter, in which the time delay between adjacent taps is chosen as 90° with respect to the frequency of operation. They report several bottlenecks for such an implementation: The rejection ratio is severly limited by dc offsets in correlators/multipliers, reference signal coupling, and duplexer group delay. However, a more fundamental limitation is that the analog LMS filter becomes unstable if the delay along the filter loop exceeds 90°. This work was reported at 835 MHz, and because of this limitation it is not possible to scale analog LMS filter to higher (5G mm-wave) frequencies.

A similar bottleneck was also observed in [64], which implemented a COTS FD

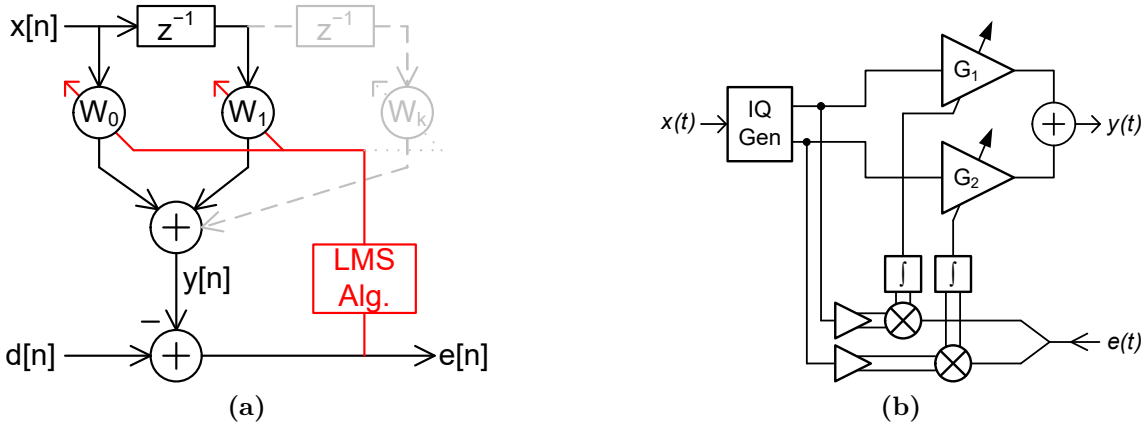


Figure 2.9: LMS adaptive filter implementations in (a) digital and (b) analog domain.

transceiver at 2.4 GHz employing RF and digital cancellation based on LMS algorithm. They manually tune the dc offset of the last stage of the canceler. Hwang [65] solves this problem by employing a digitally-controlled analog cancellation, again for a FD system at 2.4 GHz, achieving 25 dB maximum SI cancellation. The limitations of analog LMS filters are analytically derived in [66].

Either in analog or digital form, LMS algorithm alone is not sufficient on its own to realize practical FD systems. The reason is that it only removes the linear portion of the SI signal. This task is mainly performed in analog/RF domain. However, it must be combined, in the end, with nonlinear SI cancellation techniques in the digital domain. This has been recently done in [67] with COTS components at 2.1 GHz.

Adaptive filters that do not employ the LMS algorithm have also been reported [68]. It is based on a series of absolute power measurements at the RX port, after which the optimum amplitude and phase of the canceler signal is computed by geometric manipulations in approximately six iterations. This method was successfully demonstrated for a 5.8 GHz real-time transmitter leakage canceler using COTS components, but it is computationally more involved compared to analog/digital LMS implementations.

2.2.5 Self-Interference Cancellation Using Off-The-Shelf-Components

Many works can be found in the literature on low frequency (~2 GHZ) self-inteference cancellation methods utilizing COTS components. For instance, on signal-processing domain, Stimming discussed self-interference suppression methods for low-complexity full-duplex MIMO [69]. They demonstrated a 2×2 FD MIMO node at 2.48 GHz center frequency using FlexRIO 5791R RF transceiver modules, achieving 48 dB active RF suppression and 85 dB total suppression. Digital pre-distortion of power amplifiers have been proven useful in mitigating SI components in full-duplex transceivers [70], once again at 2.48 GHz using NI 5791 transceiver modules. They argue that for wideband modulated signals, the nonlinear memory effect of power amplifiers is one of the most significant limitations. They report 13 dB additional suppression attributable to predistortion. In a similar work [71], a total of 63 dB SI suppression was demonstrated from antenna and RF domains, for an 80-MHz bandwidth LTE signal at 2.46 GHz. They emphasize that nonlinear digital cancellation is necessary to push total SI suppression close to the noise floor.

Ref. [72] proposes a blind analog interference cancellation method, based on the carrier recovery techniques for BPSK signals. Thus, it is not applicable to advanced modulation techniques such as QAM.

In a recent work utilizing a single antenna configuration, the main SI leakage over the circulator is canceled using the secondary SI signals reflected from the antenna [73]. This has been achieved by modifying the frequency response of the secondary SI components using two varactor diodes at the antenna port, which can also be used to adjust the frequency band and the bandwidth. Although they reported more than 40 dB of cancellation over 65 MHz of bandwidth, the main drawback of the architecture is the power handling and nonlinear distortion of the varactor diodes for high TX powers.

2.2.6 Existing Literature in Integrated Self-Interference Canceling Transceivers

Self-interference is an issue to be dealt with, not only in full-duplex radios, but also in radios operating at close proximity, both physically and spectrally. For instance, coexistence of wireless local area networks and Bluetooth is such an example, both operating in the 2.4-GHz ISM band. In one of the early works [74], an active interference cancellation scheme is presented to combat such coexistence problems.

During the last several years, research on 5G technology has been steadily growing. Consequently, many works has focused on full-duplex radios as an enabling technology for future 5G networks. Numerous integrated transceivers has been developed featuring various self-interference cancelling schemes. In [75] a portion of the transmitted signal is coupled to a canceler network consisting of a tunable second-order RF bandpass filter, which adjusts not only the phase and amplitude of its input signal, but also the slopes of the magnitude and phase (i.e. group delay). This effectively performs frequency domain equalization. In [76], a mixer-first receive architecture is preferred. The SI cancellation is performed by a passive vector modulator downmixer consisting of 31 slices whose input is a copy of the transmitted signal. In a similar work [77], a copy of the transmitted signal is passed through analog FIR filters and fed to two

Dinc [78] uses a capacitive coupler, attenuator, amplifier, and RTPS in the canceler network of a full-duplex 60 GHz CMOS transceiver. Additionally, he proposes polarization based antenna cancellation, in which vertically and horizontally polarized slot loop antennas are used for the transmitter and receiver, respectively. He introduces an auxiliary port on the RX antenna that is copolarized with the TX antenna, and uses a reflective termination at this port. This auxiliary coupling is adjusted so that it cancels the main coupling between the antennas. As in this work, antenna domain SI suppression is common in mm-wave region. A similar slot loop antenna is employed for polarization division duplex transceiver front-end in [79], where top/bottom (vertical polarization) ports are connected to differential TX outputs, and left/right (horizontal polarization) porst are connected to differential RX

ports. The IC incorporates a similar SI canceler circuitry in the form of voltage controlled attenuators and reflective-type phase shifters.

Chapter 3

26-GHz Self-Interference Canceling Full-Duplex Transceiver Front-End in 130-nm SiGe

This chapter presents system and circuit level analysis, design, and measurement of a full-duplex transceiver front-end, implemented in a 130-nm SiGe BiCMOS process, that employs an RF self-interference canceling circuitry.

3.1 System Level Design and Analysis

The proposed full duplex front-end architecture is shown in Fig. 3.1. The blocks in red constitute the SI canceler circuit, which basically takes a copy of the transmitted signal, process its amplitude and phase to generate a canceler signal, and injects that signal to the output of the LNA. The blocks in blue consitude the low-power IQ downconversion functionality, the baseband/dc outputs of which can be used to monitor the amount of correlation between the transmitted and received signal. This information can be used to adaptively determine the optimum phase and amplitude control settings of the canceler.

The main application of such an RF SI cancellation technique is to mitigate only the main leakage from TX to RX, which is either over the duplexer (EBDs or ferrite

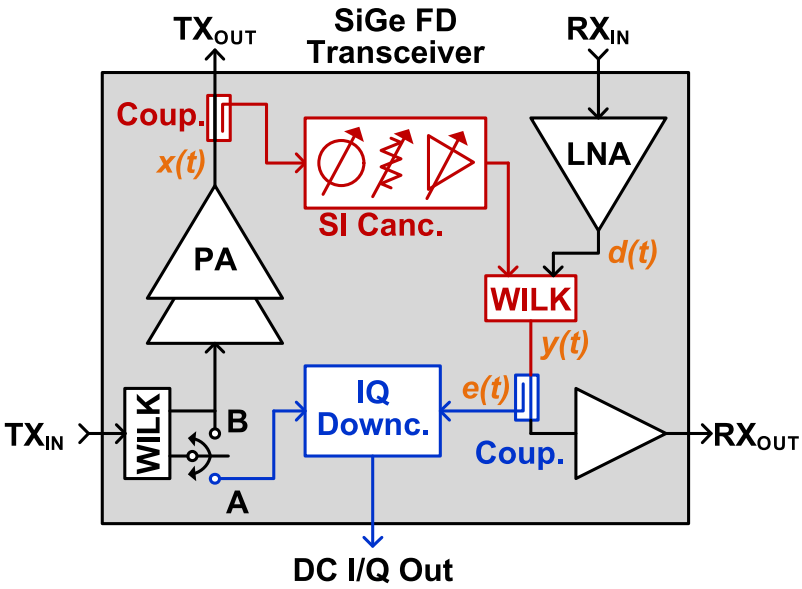


Figure 3.1: Block level view of the proposed full-duplex transceiver architecture.

circulators) or over the shared antenna interface. SI signals that reflect from the environment are order of magnitude smaller compared to the main SI signal, and to cancel/suppress them effectively requires not only phase adjustment, but also delay adjustmet. The main SI component does not change as fast as the power profile of the SI component due to environmental reflections. With this motivation, a switchable Wilkinson is introduced to the TX_{IN} port that may be used to disable the IQ downconversion functinality once the optimum amplitude/phase settings are obtained. This method improves TX radiated power about 2.5 dB.

In this part, first the effect of phase and amplitude control resolution on cancellation performance will be investigated, followed by a discussion on RX linearity requirements for sufficient SI cancellation performance. The following discussion is valid, though, for any RF self-interference cancellation scheme that employs phase/amplitude control based cancellation circuitry.

3.1.1 Phase and Amplitude Control Resolution

Assume that the canceler consists of a phase shifter with phase steps of ϕ radians and a linear-in-dB attenuator with steps of $20 \log A$ dB. The worst case scenario is when the ideal canceler signal (inverse of the interferer) is equidistant to the nearest four constellation points that can be generated by the phase/amplitude control

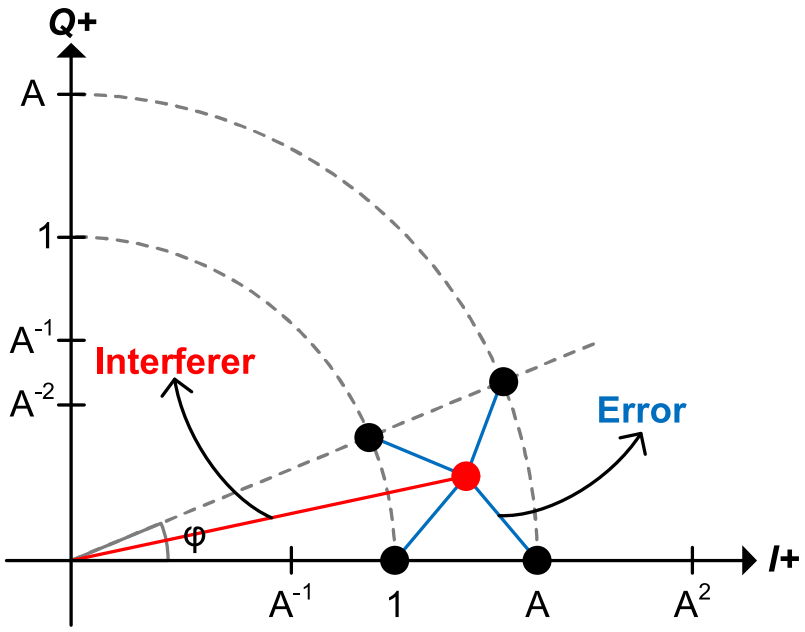


Figure 3.2: Phasor diagram displaying the canceller and error signals with respect amplitude and phase control resolution.

blocks. This situation is visually depicted in Fig. 3.2. In this scenario, without loss of generality, the interferer and error signals can be expressed as

$$\text{Int} = \frac{A+1}{2\cos(\phi/2)} e^{j\phi/2} \tag{3.1}$$

$$\text{Err} = \frac{A+1}{2\cos(\phi/2)} e^{j\phi/2} - 1 \tag{3.2}$$

Therefore, the amount of SI cancellation can be calculated as

$$\text{SIC} = \frac{\left|\text{Err}\right|^2}{\left|\text{Int}\right|^2} = \frac{\left|(A+1)e^{j\phi/2} - 2\cos(\phi/2)\right|^2}{\left|A+1\right|^2} = \frac{1+A^2-2A\cos\phi}{1+A^2+2A} \tag{3.3}$$

The above equation means that an ideal 6-bit phase shifter (5.6° steps) and a 0.5 dB step attenuator can ideally achieve 25 dB SI cancellation. To achieve 30 dB SI cancellation, a 7-bit phase shifter (2.8° steps) and a 0.25 dB step attenuator are required, resulting in 31 dB SI cancellation. The contours of SI cancellation for various phase/amplitude control bit resolutions are shown in Fig. 3.3.

In reality, phase/amplitude control blocks exhibit nonideal behavior in terms of phase/amplitude step size between their different states. These are often specified by the rms value of the error, for instance for phased array systems. However, here

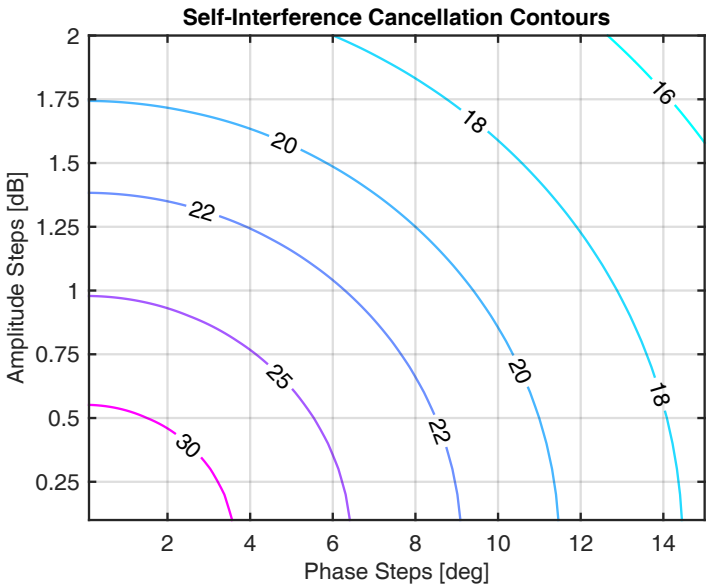


Figure 3.3: Contours of self-interference cancellation versus amplitude (y-axis) and phase (x-axis) control resolution.

we are interested in the worst case SI cancellation performance. Hence, rather than rms errors we are interested in the maximum error between any adjacent states. To make it clear, this is analogous to the maximum DNL (differential nonlinearity) of an ADC (analog-to-digital converter). In this context, the step sizes in Fig. 3.3 or in (3.3) must be understood not as the nominal resolution of the phase shifter or attenuator, but as the maximum step size between their adjacent states.

Due to device mismatches and process variations it is practically impossible to achieve >7-bit phase shifters. However, in the case of adaptive SI cancellation it is not necessary to realize an accurate >7-bit phase shifter. The only requirement is to achieve a worst case phase shift step of 2.8°. In order to achieve this, this work utilizes a 10-bit IQ modulator as the phase shifter portion of the canceler.

The very first 10-b phase shifter targeting duplexing applications was demonstrated by Amirkhanzadeh, but it operates at low frequencies of 1.8-2.4 GHz, it was fabricated in a costly silicon-on-saphire (SOS) process, and the die size is very large at 5.94 mm^2 [80].

3.1.2 RX Linearity Requirements

Suppose the input signal of the LNA is of the form $x(t) = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t$. If the LNA gain is modeled as a third degree polynomial, $G(x) = ax + bx^2 + cx^3$, the output signal of the LNA can be found as

$$\begin{aligned} y(t) &= aA_1 \cos\omega_1 t + aA_2 \cos\omega_2 t \\ &+ \frac{bA_1}{2}(1+\cos 2\omega_1 t) + \frac{bA_2}{2}(1+\cos 2\omega_2 t) + A_1A_2\big(\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t\big) \\ &+ cA_1^3\left(\cos\omega_1 t + \frac{\cos 3\omega_1 t}{2}\right) + cA_2^3\left(\cos\omega_2 t + \frac{\cos 3\omega_2 t}{2}\right) \\ &+ cA_1^2A_2\left(\frac{\cos\omega_2 t}{2} + \frac{\cos(2\omega_1+\omega_2)t}{4} + \frac{\cos(2\omega_1-\omega_2)t}{4}\right) \\ &+ cA_1A_2^2\left(\frac{\cos\omega_1 t}{2} + \frac{\cos(2\omega_2+\omega_1)t}{4} + \frac{\cos(2\omega_2-\omega_1)t}{4}\right) \end{aligned} \tag{3.4}$$

In FDD/TDD systems we suppose that ω_1 and ω_2 are closely-spaced and proceed to define linearity metrics such third-order intercept point. However, in the extremes of full-duplex communications, they can be equal to each other; one representing the desired received signal and the other representing the unwanted self-interference from the transmitter. For both cases we are only interested in the signal components that are *near* the excitation frequencies. Hence, neglecting the higher and lower frequency components and rearranging the terms we find that

$$\begin{aligned} y(t) = aA_1\cos\omega_1 t + aA_2\cos\omega_2 t + c\left(A_1^3 + \frac{A_1A^2}{2}\right)\cos\omega_1 t + c\left(A_2^3 + \frac{A_1^2A_2}{2}\right)\cos\omega_2 t \\ + \frac{cA_1^2A_2}{4}\cos(2\omega_1-\omega_2)t + \frac{cA_1A_2^2}{4}\cos(2\omega_2-\omega_1)t. \end{aligned} \tag{3.5}$$

The first two terms in (3.5) are the amplified versions of the input signal, as $a > 1$ for an amplifier. The third and fourth terms represent gain compression at high input powers as c is negative in typical class-A amplifiers (they do not exhibit any gain expansion at high input power). The last two terms are the inter-modulation distortion (IMD) products that appear very close to the input frequencies.

In the context of full-duplex communications we have $\omega_1 = \omega_2$. Suppose that A_1 and A_2 represent the amplitudes of the received signal and the self-interference

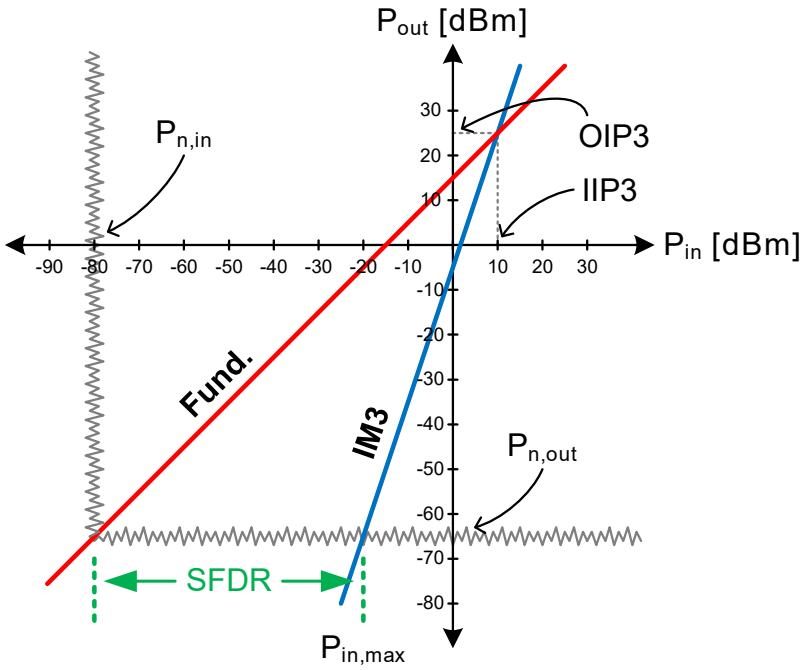


Figure 3.4: Linearity analysis of the receiver.

signal, respectively. Note that $A_2 \gg A_1$ for almost all cases. This is not a problem in FD systems as long as the LNA output signal, $y(t)$, is free from IMD products. In such a case, the known TX signal can be subtracted from the received signal either in analog or digital domain. Of course, this ideal scenario is practically limited by many nonidealites, such as TX and RX oscillator phase noise, multiple reflections of the TX signal from the environment, the time varying nature of the wireless channel etc., but these are challenges that have to be tackled anyway. However, FD operation is not feasbile, *if* the LNA output exhibits IMD products of the SI signal. As they are at the very same frequency (last two terms of (3.5)) and not known by the transmitter, they are not different from a desired signal from the receiver's perspective, and therefore cannot be cancelled in analog or digital domain. The problem is more severe in actual FD communication systems, since the transmitted signal is not a single tone sinusoid as in the case discussed above. It is a modulated signal occupying tens or hundreds of MHz bandwidth, creating complex and hard-to-characterize IMD products, which completely mask the desired signal. Therefore, it is essential that the LNA (the complete receiver actually) is sufficiently linear and that the output of the LNA is free from such SI intermodulation products.

The above discussion explains the trade-off between the TX output power, RX

linearity, and passive antenna isolation. This can be visually understood in Fig. 3.4. Here, the fundamental tone refers to the SI signal and IM3 refers to its third-order intermodulation product. The power at the LNA input must be limited to a certain value $P_{in,\max}$ so that SI IM3 components are below the noise floor, i.e. the LNA must operate within its spurious-free dynamic range (SFDR). This value can be found as follows. The IM3 curve in Fig. 3.4 can be expressed as

$$P_{out} - \mathrm{OIP}_3 = 3(P_{in} - \mathrm{IIP}_3), \tag{3.6}$$

which can be rewritten as

$$P_{out} = 3P_{in} - 2\mathrm{IIP}_3 + G. \tag{3.7}$$

Then setting $P_{out} = N_{out}$, the noise floor at the LNA output, we can find the maximum allowed signal at the LNA input.

$$P_{in,\max} = \frac{N_{in} + 2\mathrm{IIP}_3}{3} \tag{3.8}$$

Note that here N_{in} includes the noise figure of the LNA, i.e. $N_{in} = kTBF$ in linear terms, where k is the Boltzmann's constant, T is the absolute temperature in Kelvin, B is the bandwidth and F is the noise factor. We can further relate this maximum allowed signal to the transmitted power (P_{TX}) and passive antenna isolation from TX to RX (C_{TX-RX}), since we must satisfy $P_{in,\max} < P_{TX} + C_{TX-RX}$.

To better appreciate the trade-off, the following case study has been made. At 5G mm-wave bands (26/28 GHz) a typical LNA in SiGe BiCMOS achieves 10 dBm OP1dB. For class-A operation this means an OIP3 of approximately 20 dBm. For a typical LNA gain of 15 dB, we have $\mathrm{IIP}_3 = 5$ dBm. The complete receiver may have a noise figure of 5 dB. For 100 MHz bandwidth, noise floor at LNA input becomes $-174 + 5 + 10\log(100 \times 10^6) = -89$ dBm. Combining these results we have $P_{in,\max} = \frac{-89+2\times5}{3} = -26.3$ dBm. Therefore, for 15 dBm TX output power, typical in this frequency range and process, we would require 41.3 dB passive antenna

suppresion of the SI signal. Passive suppression more than 40 dB is challenging, especially at mm-wave frequencies. Thus, for such an FD communication link to operate, TX output power may be reduced (range would be smaller), RX linearity may be improved (LNA small-signal linearization techniques can be utilized or more current can be consumed for improved linearity), or modulation bandwidth may be increased. Increasing the modulation bandwidth eases LNA linearity requirement, but makes the analog/digital SI cancellation much harder.

3.2 10-b Vector Modulator Phase Shifter

This section presents a high resolution (10-b) vector modulator (VM) in 130-nm SiGe BiCMOS to achieve high self-interference cancellation performance in 26 GHz full-duplex 5G applications. The design employs the Gilbert-cell topology, an 8-b on-chip current-steering DAC to control its tail currents, a 2-b I/Q sign switches, an on-chip PTAT current reference, and a process compensation circuitry.

The design of the vector modulator can be divided into RF circuitry and dc/control circuitry, as shown in Fig. 3.5. The RF part includes a transformer balun, an RC polyphase filter (PPF) quadrature generator, and Gilbert-cell type vector modulator; and the dc design part includes a PTAT current reference, process compensation circuitry, current steering DAC, and cascode tail current source.

3.2.1 Transformer Balun

In order to achieve high linearity, the vector modulator uses a transformer balun instead of an active balun. Transformer baluns are widely utilized at RFICs and well studied [81]. At 26 GHz, transformer baluns are considerably small compared to transmission line based baluns. The design can be seen in Fig. 3.6. It converts a single-ended 50 Ω to differential 100 Ω. The 200 pH primary coil was realized by a single turn top-metal 2 trace of width 12-μm and inner diameter of 80-μm. The 440 pH secondary coil was realized by a two-turn top-metal 1 trace of width 10-μm and inner diameter of 43-μm. This geometry produces a moderate magnetic coupling

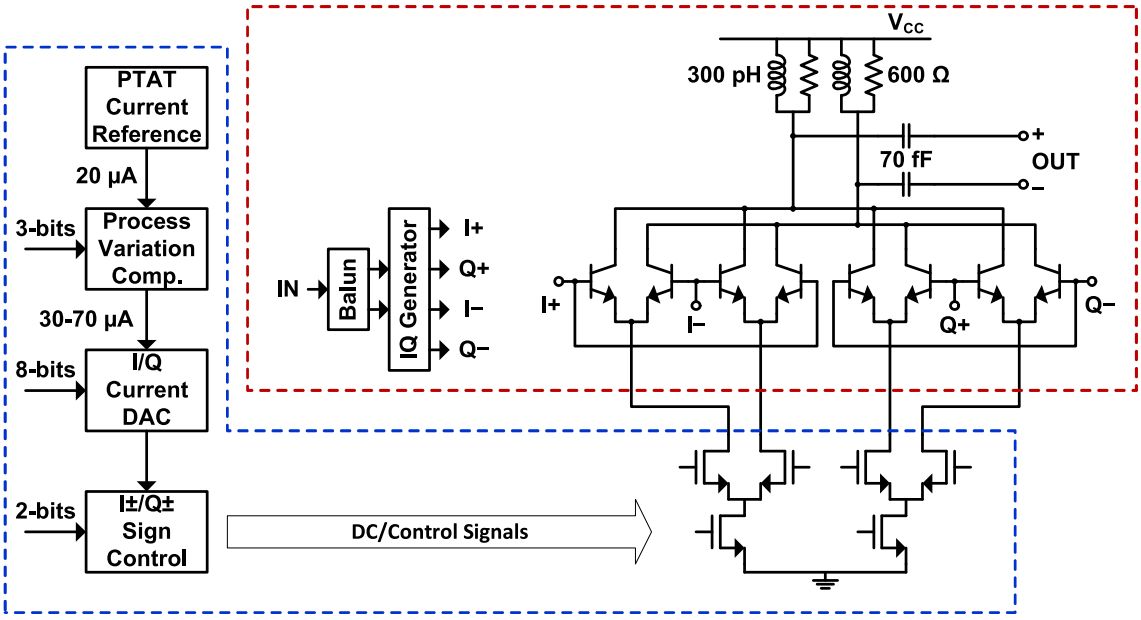


Figure 3.5: The architecture of the process-compensated high-resolution (10-b) vector modulator. Red box: RF part, blue box: dc/control part.

coefficient of $k = 0.59$ to enable a wideband matching performance. It was optimized to maximize the available power gain of the transformer. The 150 fF and 40 fF MIM capacitors tune out the inductance of the coils and perform the matching. Two 80 fF capacitors are used in series to realize the 40 fF capacitor, while ensuring the symmetry. The overall balun has a simulated insertion loss of 1.2-1.5 dB in 25-30 GHz band, and its phase/amplitude imbalance is less than 0.4°/0.35 dB.

3.2.2 I/Q Generator

There is a vast literature on different techniques of quadrature signal generation [82–87]. The balun is followed by a 2-stage RC polyphase filter. Its advantages are good amplitude and phase balance between its outputs, high linearity, and very compact area; and its main disadvantage is insertion loss. A quadrature all-pass filter (QAPF) could have been used instead, providing significantly less insertion loss, but we preferred phase/amplitude balance advantage of the 2-stage PPF over the insertion loss advantage of QAPF. We used the constant amplitude configuration of the 2-stage RC PPF as shown in Fig. 3.6, where $R = 100\ \Omega$ and $C = 57$ fF. The actual layout implementation is slightly different than the schematic drawing to ensure symmetry and utilizes dummy resistors and capacitors for better device

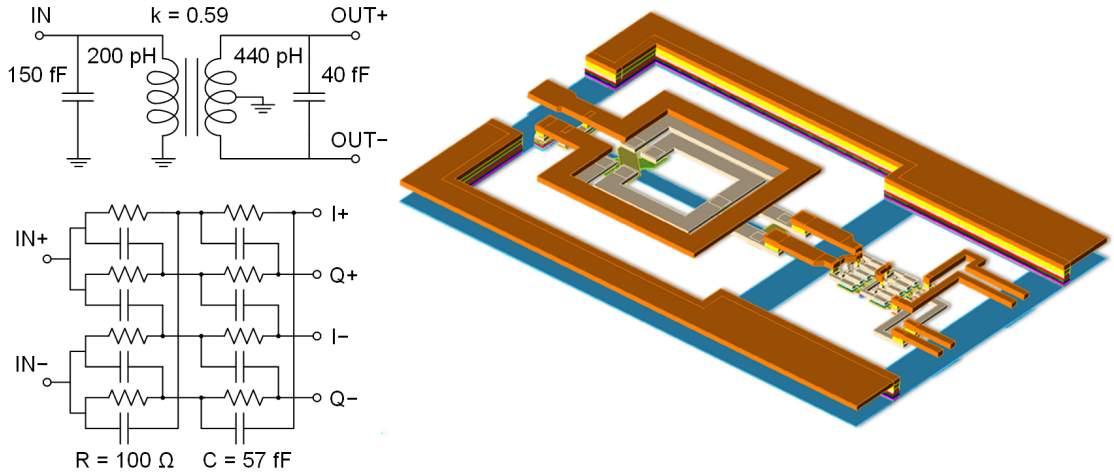


Figure 3.6: Schematic and 3D layout views of the transformer balun and the 2-stage RC polyphase filter.

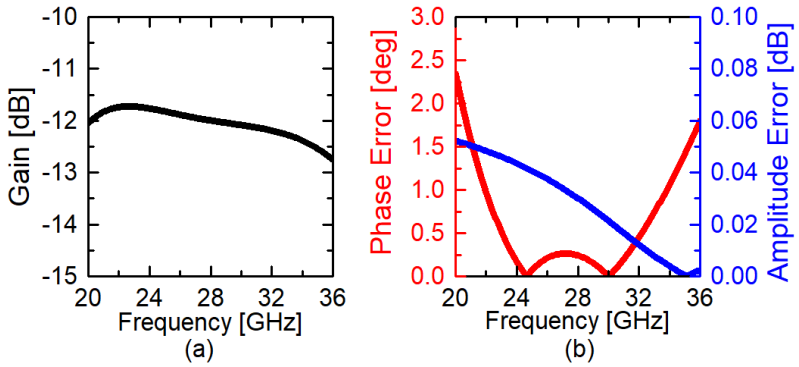


Figure 3.7: The simulated (a) gain and (b) phase/amplitude imbalance of the cascaded transformer balun and 2-stage RC polyphase filter.

matching.

Fig. 3.7 shows the EM simulation results of the cascaded balun and quadrature generator. The total insertion loss is 12 dB at 26 GHz and input/output return losses are better than 10 dB from 20 to 36 GHz (not shown here). By tuning the line lengths after the 2-stage PPF, the phase error was adjusted to exhibit two zero-crossings that were placed on separate sides of 26 GHz, as can be seen in Fig. 3.7(b), to maintain a good phase balance between the outputs even under process variations. The phase error is less than 1° in 22-34 GHz band and the amplitude error is negligible, as the RC PPF is used in the constant-amplitude configuration.

3.2.3 Gilbert-Cell Core

Differential I and Q signals of the PPF are fed to the core of the vector modulator as shown in Fig. 3.5. The HBT sizes are 8×0.48 μm and they are biased for a maximum tail current of 7.5 mA. The HBT sizes are chosen to provide a trade-off between power consumption and RF output power. The 300 pH shunt inductor and 70 fF series capacitor form the output matching network for a 100 Ω differential load, and a 600 Ω resistor is used to widen the output matching bandwidth. This type of modulator has the benefit of a constant power consumption that is independent of its setting and input drive power, unlike the current steering type modulators whose power consumption changes as a function of the phase setting. The tail current of the HBTs are provided by NMOS transistors. The bottom NMOS acts as a current source and the upper ones act as a sign switch for I and Q signal paths.

3.2.4 Reference Current Generation With Process Compensation Capability

The performance of a high-resolution vector modulator strongly depends on its dc bias and control voltages. In this work, to tolerate process and temperature variations, dc bias and control voltages are generated by on-chip circuit blocks: a PTAT current reference followed by a 3-b process compensating PMOS current mirror, an 8-b current-steering DAC, and a cascode current mirror with 2-b sign switches.

The on-chip PTAT current reference has a nominal output current of 12 μA at room temperature. It draws 720 μA from a 2.5 V supply for a power consumption of 1.8 mW.

To compensate for possible process variations, a PMOS cascode current mirror with 3-b control capability was employed, as seen in Fig. 3.8. In nominal operation only the MSB of the three bit control word is high. The output current of this stage is in the range of 16-26 μA, i.e. a 21 μA nominal current with $\pm$25% tunable range, as can be seen in Fig. 3.9. The output current is constant up to a load voltage of

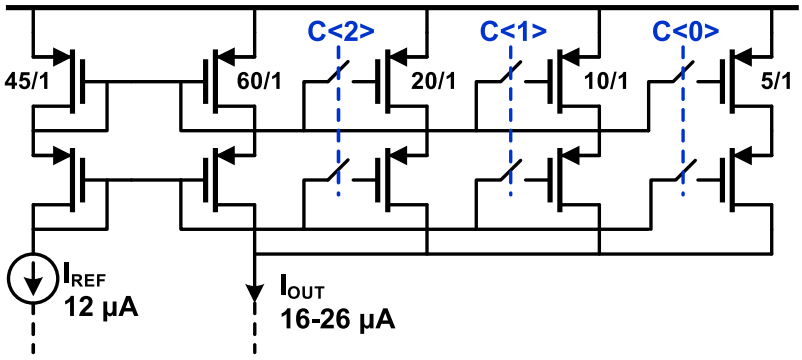


Figure 3.8: Schematic view of the PMOS cascode current mirror with 3-b process compensation capability.

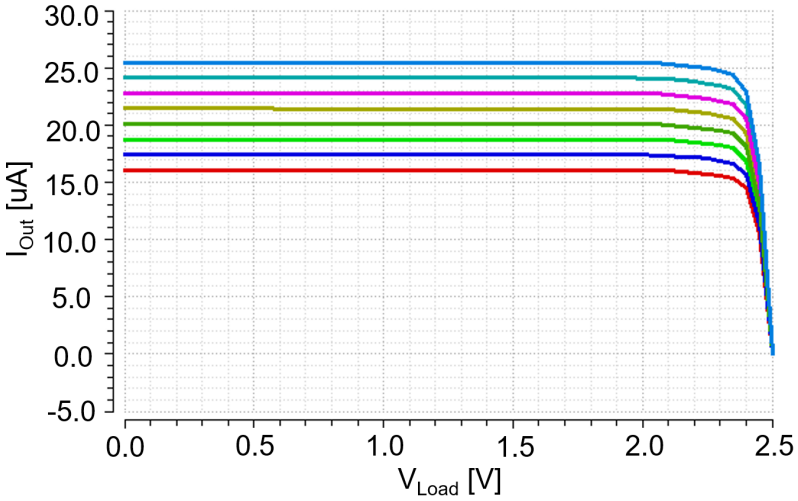


Figure 3.9: Simulated output current of the process compensating PMOS current mirror.

2.3 V, which is more than enough.

3.2.5 Current-Steering DAC

The critical part of the dc/control circuitry is the current steering DAC. It is based on cascode PMOS current steering topology, as shown in Fig. 3.10. The sizes of PMOS transistors in each DAC cell are binary weighted between $W/L = 2.5\mu\text{m}/0.5\mu\text{m}$ and $320\mu\text{m}/0.5\mu\text{m}$. The largest possible device sizes are used that allow less than 10 ns settling time. We chose almost 4 times the minimum gate length of the process, to minimize the effects of process variations, since monotonicty is the primary goal. The long channel devices ($L = 0.5$ μm) help increase the linearity of the DAC. The maximum output current of the DAC is 500 μA. The change in the output current of the DAC is shown in Fig. 3.11 as a function of load voltage. Only

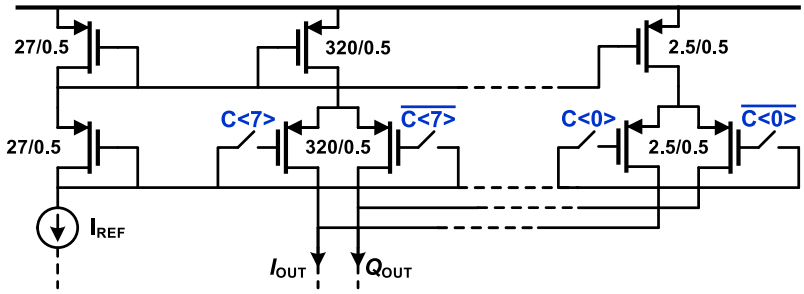


Figure 3.10: Schematic view of the 8-b, PMOS, binary-weighted, current-steering DAC.

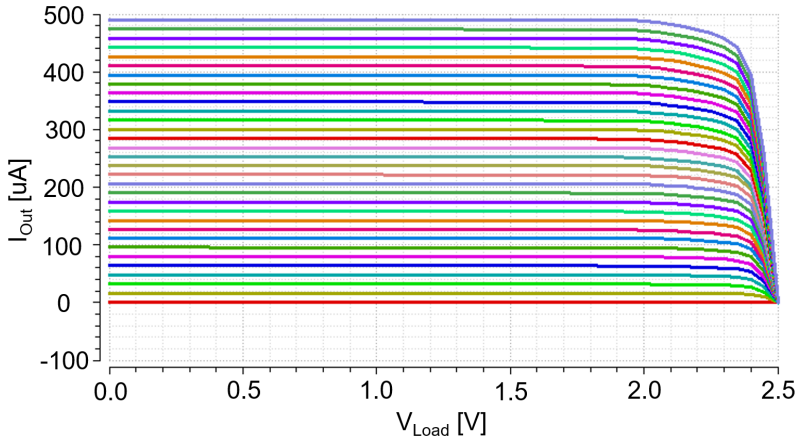


Figure 3.11: Current values at one of the outputs of the current-steering DAC vs. the load voltage. Different colors show the output currents for the swept 5 MSB of the DAC control word.

the 5 most significant bits were swept for better visibility.

3.2.6 I/Q Sign Switches and Tail Current Mirrors

The final part of the dc/control circuitry is NMOS cascode current mirrors to provide the tail currents of the Gilbert-cell type vector modulator, as shown in Fig. 3.12. Here, M_5 and M_3 form a current mirror that operate from a reference current ranging from 0 to 500 μA maximum. Depending the one desired quadrature of the vector modulator, one of the I_+ or I_- (similarly Q_+ or Q_-) paths is enabled and the other one is disabled, using the IQ sign switches (M_{6-9}), which are implemented in series-shunt SPDT configuration. This topology is superior to using only series switches in terms of switching speed, as the gate of M_1 or M_2 (the path that is disabled) is pulled down to ground when that path is disabled. The common-source transistors are sized 10μm/0.5μm and 150μm/0.5μm, and the common-gate

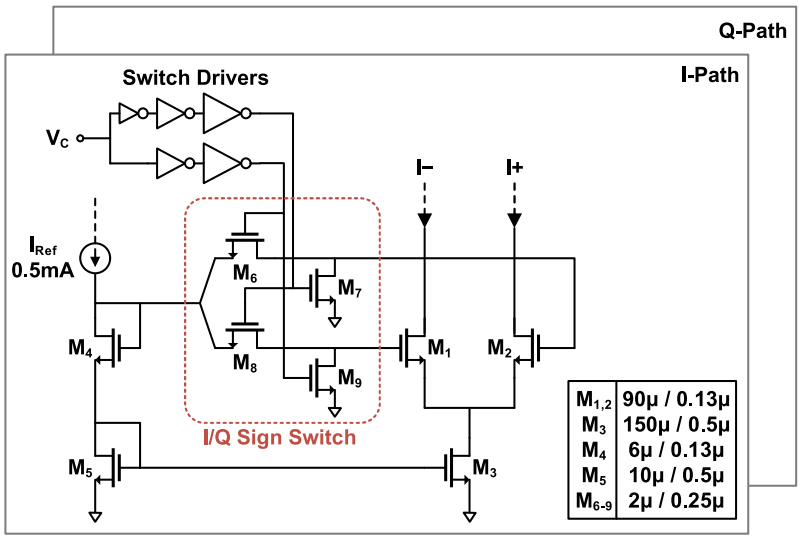


Figure 3.12: Schematic view of the I/Q tail current mirrors.

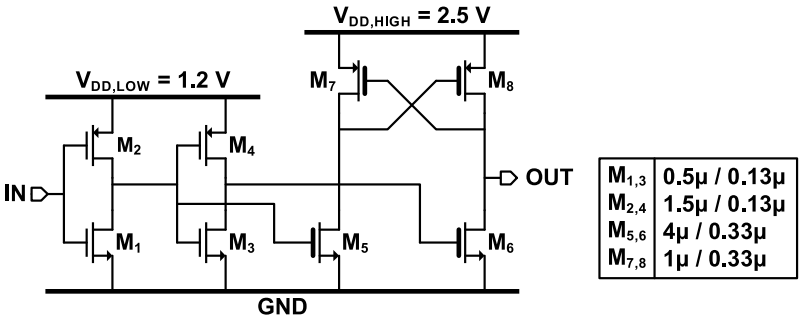


Figure 3.13: Schematic view of the level shifting switch driver.

transistors are sized 6μm/0.13μm and 90μm/0.13μm, to provide a maximum tail current of 500 μA $\times$ 15 = 7.5 mA.

Finally all the switches in the I/Q DAC discussed so far was controlled with a 0/2.5 V digital signals. However, the digital libraries in the process is offered for 1.2 V operation. The control signals of the I/Q DAC comes from the on-chip SPI that custom designed by my colleague Abdurrahman Burak. Therefore we need driver circuitry for all these switches. We adopted the topology shown in Fig. 3.13. $M_{1–4}$ are low-V_T devices that function as the input inverting buffers, driving the gates of $M_{5,6}$, which are high-V_T devices. Drains of these devices are connected to the cross-coupled PMOS pair $M_{7,8}$. These are weak devices so that their drains can be pulled down by $M_{5,6}$, when a low-to-high transition occurs at their gates.

The overall layout of the complete control circuitry of the vector modulator is shown in Fig. 3.14. It occupies a die area of 0.17×0.2 mm^2.

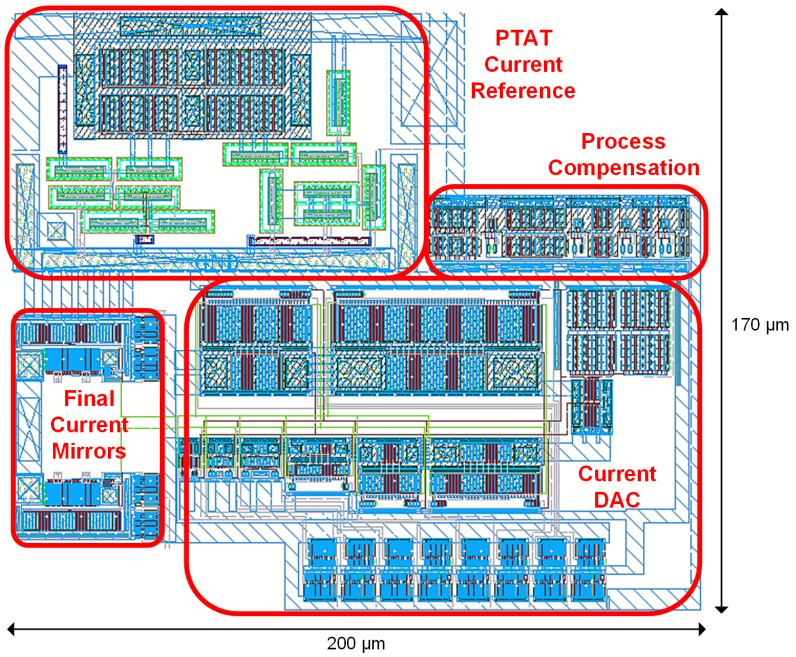


Figure 3.14: Final layout of the DC/control circuitry of the IQ modulator.

3.2.7 Measurement Results

The vector modulator is fabricated in IHP SG13S BiCMOS technology (see Appendix A for process details). The chip micrograph is shown in Fig. 3.15. It includes input/output baluns for single-ended measurements. The IC also features a custom-designed SPI for the 10-b phase control and 3-b process compensation controls. All digital pads include ESD protection circuitry. The chip area is $0.8 \times 0.6 = 0.48$ mm^2, excluding the pads; and the core area is $0.4 \times 0.6 = 0.24$ mm^2, excluding the baluns.

The pad-to-pad S-parameters are measured with a PNA N5224A network analyzer and an RF probe station, using the setup shown in Fig. 3.16 and 3.17. 100-um GSG Z-probes are used for the input/output RF connections, and the supply/digital controls are provided by a GGB dc probe.

Fig. 3.18 shows the measured insertion gain across different phase settings. After deembedding the combined 3 dB loss of the input/output baluns that were separately fabricated and measured, the average loss of the vector modulator is around 0.5 dB, with an rms gain error of 0.3 dB. Input/output of the PS is well-matched to 50 Ω, as seen in Fig. 3.19, which is predominantly determined by the baluns. The measured

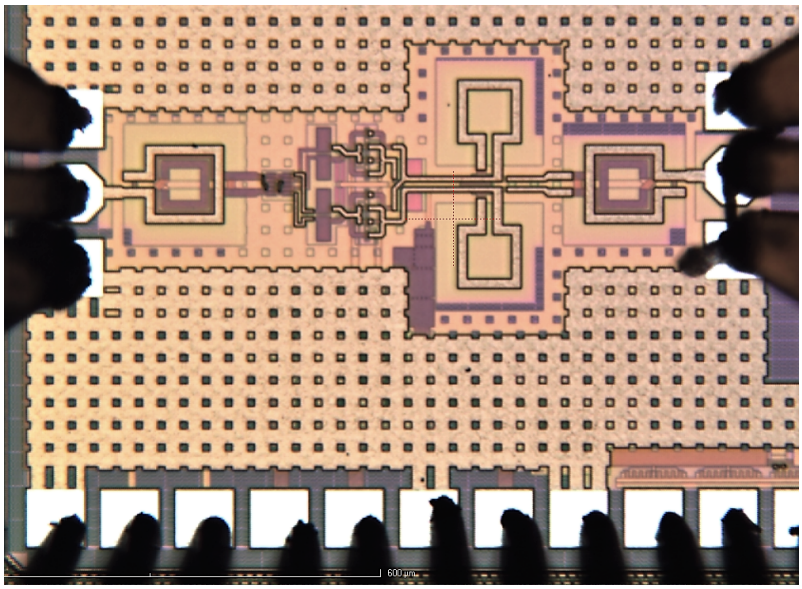


Figure 3.15: Die photo of the vector modulator.

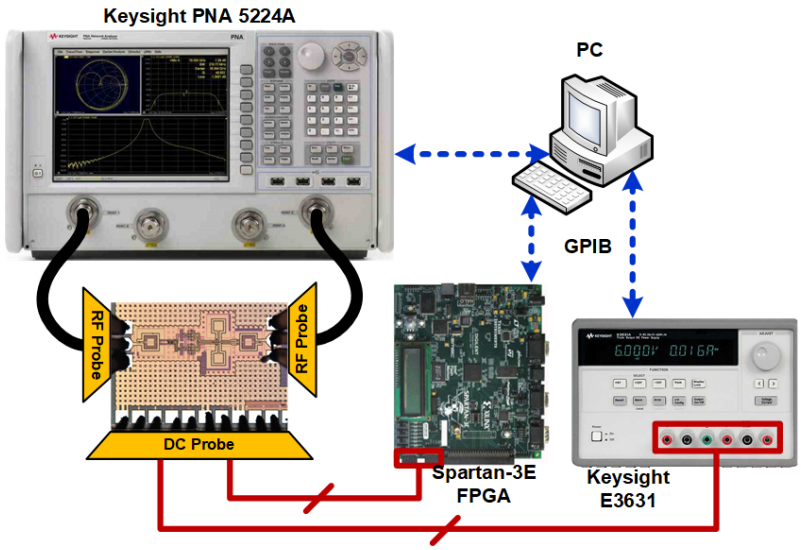


Figure 3.16: Measured relative phase shifts of the VM for different states. Only 32 major states are shown for clarity.

group delay is around 40 ps at 26 GHz center frequency (not shown here).

Fig. 3.20 shows the relative insertion phase across different phase settings. Here, only the 5-MSB control is swept to display the phase shifts for brevity and clarity. These results are obtained without any phase calibration. Note that, these phase shifts do not correspond to an ideal 5-b phase shifter, since the DAC in this work was implemented in a binary fashion. They must be properly weighted to synthesize an N-bit phase shifter [88]. Nevertheless, if these phase states are treated as the states of a 5-b phase shifter, the VM achives 4-5° rms phase error without any calibration.

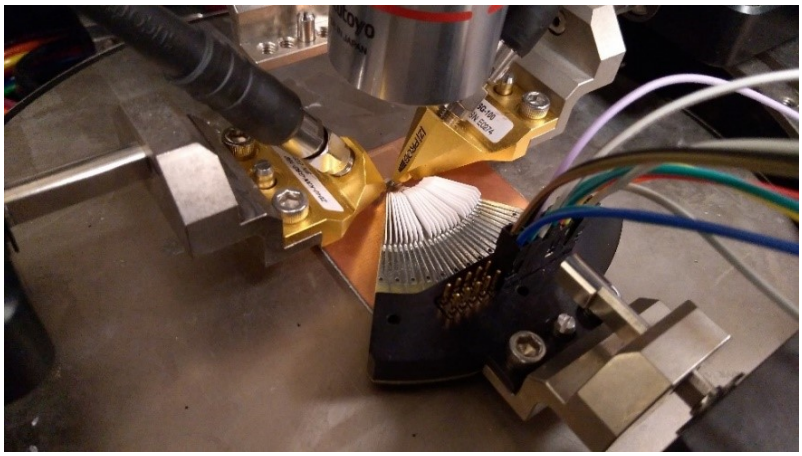


Figure 3.17: Measured gain of the VM for all states.

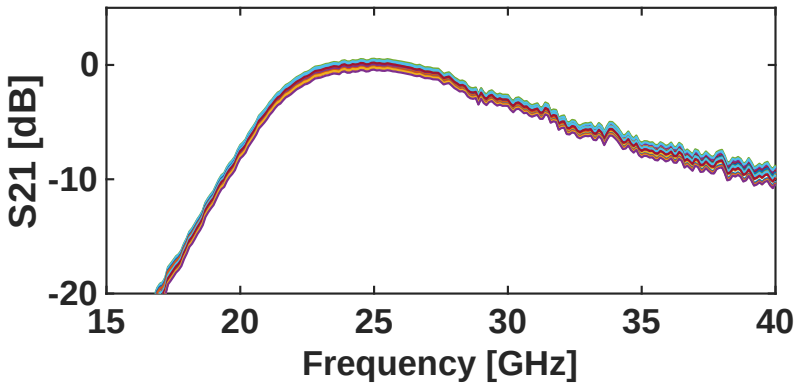


Figure 3.18: Measured input and output matching for all phase states.

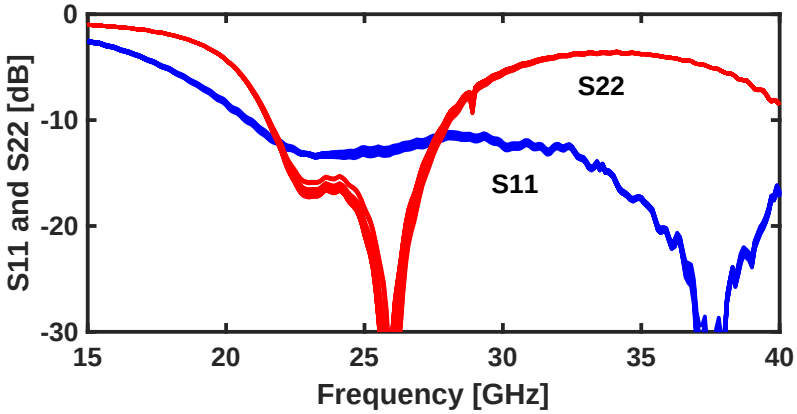


Figure 3.19: Measured input and output matching for all phase states.

The other 5-LSB controls can easily be used to improve the performance the phase shifter. For instance, we were able to synthesize an 8-b phase shifter with 0.2° rms phase error, which is a state-of-the-art performance.

Our aim in this work was to obtain perfectly monotonic phase states. We measured all the $2^{10} - 4$ phase states, and observed perfectly monotonic phase shifts,

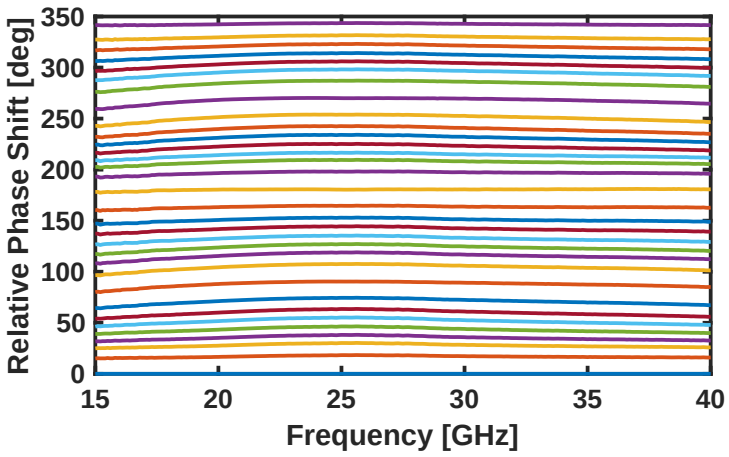


Figure 3.20: Measured relative phase shifts of the VM for different states. Only 32 major states are shown for clarity.

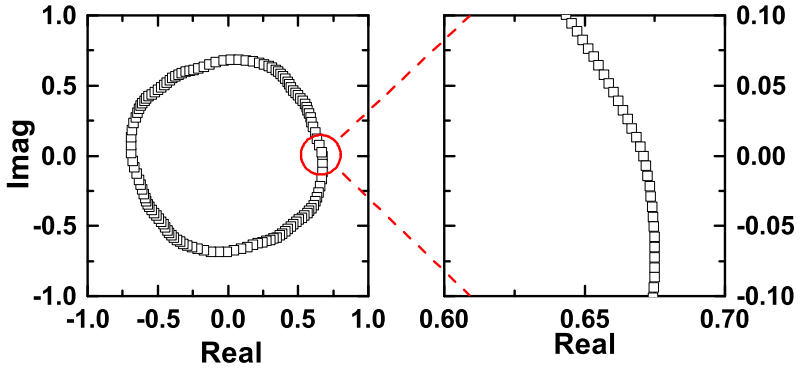


Figure 3.21: Measured constellation of S21 at 26 GHz. (Left) One out of eights states is shown for brevity. (Right) Zoomed in version showing all the states

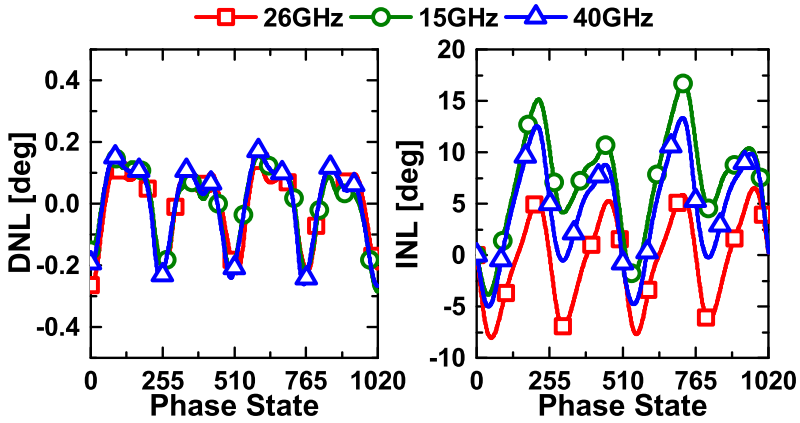


Figure 3.22: Measured INL and DNL for the vector modulator.

without any dead zones from 0 to 360°. (-4 is due to the four redundant phase states in $I_{\pm}/Q_{\pm}$ transitions). Fig. 3.21 shows the S21 constellation, and its zoomed-in version. The measured worst case (largest) phase difference between any adjacent

Table 3.1: Comparison of State-of-The-Art Silicon-Based Vector-Modulators at 26-28 GHz

Reference	**This Thesis**	[29]	[39]	[89]	[90]
Technology	**130nm SiGe**	180nm SiGe	130nm SiGe	130nm CMOS	180nm CMOS
Phase Resolution	**8-b/5-b**	6-b	4-b	6-b	4-b
Phase Err. [°rms]	**0.2/4**	3.4	5.4	2.6	1.5
Gain [dB]	**−0.5**	1	10.5	−5	−15
Gain Err. [dB rms]	**0.2**	0.5	0.6	0.31	0.45
NF [dB]	**17**	12	7	18	15
IP_{1dB} [dBm]	**2**	−7	−17	−10	12
P_{DC} [mW]	**23**	-	136	27	0
Chip Area [mm^2]	**0.45**	-	0.3	0.3	0.31

states is 0.65°. As would be expected and can be seen in the figure, these largest gaps occur around the quadrature reference vectors.

Fig. 3.22 shows the DNL and INL of the VM for each 1020 control code, at three different operating frequencies, treating the VM as a digital-to-phase converter. For almost all control codes, the measured DNL is between ±0.2° and its worst case value is −0.3°, meaning the phase states are completely monotonic. The best INL performance is obtained at the center frequency (between +5° and −8°) and it degrades further for higher/lower frequencies. This INL performance was expected, though, since the DAC cells were binary weighted. *This vector modulator does not provide absolute phase accuracy, however, it achieves perfectly monotonic 10-b phase states.* The implication is that this vector modulator cannot be used as an accurate RF "phase shifter", such as phased array beamformer channels presented in the next chapter. The target application of this work is high-performance self-interference cancellation in full-duplex radios, which requires good DNL but not necessarily INL.

The vector modulator core draws 7.5 mA current from a 2.5 V supply, and the total power consumption is 23 mW including the dc biasing and control circuitry (DAC 2.5 mW and PTAT reference 1.5 mW). The linearity of the vector modulator was characterized with single-tone measurements. The VM has an input-referred 1-dB compression point (IP1dB) of +2 dBm. Finally, the noise figure of the VM

Table 3.2: The Effect of 4-b Process Compensation Control of the Vector Modulator on the DC Current and Gain/Phase at 26 GHz.

Cont. Word	I_{DC} [mA]	Gain [dB]	Phase [deg]
0001	0.4	9	−3
0010	0.8	15	−39
0011	1.3	18	−41
0100	1.7	20	−43
0101	2.1	21	−45
0110	2.5	22	−46
0111	2.9	23	−47
1000	4.8	25.8	−49
1001	5.2	26.2	−50
1010	5.6	26.5	−51
1011	6.0	26.8	−52
1100	6.3	27.0	−52
1101	6.7	27.2	−53
1110	7.1	27.4	−53
1111	7.5	27.6	−54

is quite high at 17 dB, mainly due to the losses of the 2-stage RC polyphase filter, however, this is not a concern, since this vector modulator will be used in a self-interference cancellation circuitry that will operating on a copy of the transmitted signal with a high signal-to-noise ratio (SNR).

For completeness, Table 3.1 compares state-of-the-art silicon VMs at 26/28 GHz band. Two versions are included in the table for this work. The 5-b version represents the uncalibrated PS performance obtained by sweeping only the 5-MSBs (Fig. 3.20), without using the other 5-b control. The 8-b version represents the PS that was synthesized after measuring all the phase states. The presented work achieves the highest phase resolution and linearity (as [90] is fully passive), the lowest rms phase/gain error, and comparable performance in other aspects.

Finally, the process compensation capability of the dc/control circuitry of the vector modulator was tested. The results are shown in Table 3.2

3.3 Low-Power I/Q Downconverter

Initially, our motivation was to employ a power detector to find the magnitude of the error signal, $e(t)$, in Fig. 3.1. Power detectors in SiGe can be easily implemented

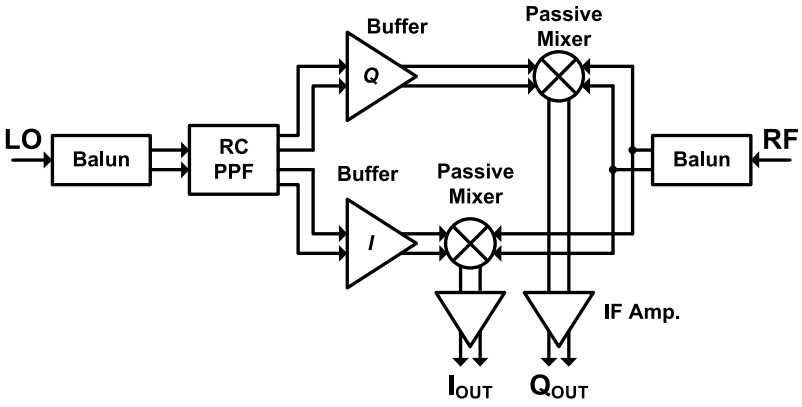


Figure 3.23: Low-power IQ downconverter system architecture.

with nonlinear I-V characteristic of the base-emitter junction. However, this type of detection suffers from dynamic range issue [91–93], typically achieving dynamic ranges on the order of 25 dB. Targeting more than 30 dB RF SI cancellation, combined with 30 dB passive antenna suppression would necessitate a power detector having more than 60 dB dynamic range.

A distributed power detection scheme was briefly considered, in which, a series of N power detectors are used simultaneously, with their inputs properly offset from one another by amplifiers having a gain of 16 dB. The operation is analogous to that of logarithmic amplifiers. Using four power detectors in this configuration, the combined dynamic range could have been extended to $25 + 3 = 73$ dB. However, the implementation occupied exceedingly large die area, comparable to the complete transceiver size itself.

With this motivation, the IQ downconversion system shown in Fig. 3.23 has been developed. The operation, within the full-duplex transceiver IC will be as follows: One of the outputs of the switchable wilkinson at the $\mathrm{TX_{IN}}$ port can be connected to the IQ downconverter, so that the transmitted signal can be used as the LO signal for the downconversion. This of course necessitates the transmitted signal to be continuous, single tone, sinusoidal signal, not a modulated wideband signal. Therefore, it is envisioned that the IQ downconverter will be operating in the foreground for calibration purposes.

The coupled signal from the RX output in Fig. 3.1 is the RF signal in Fig. 3.23. A singl-estage RC PPF is used to generate IQ signals, followed by differential LO

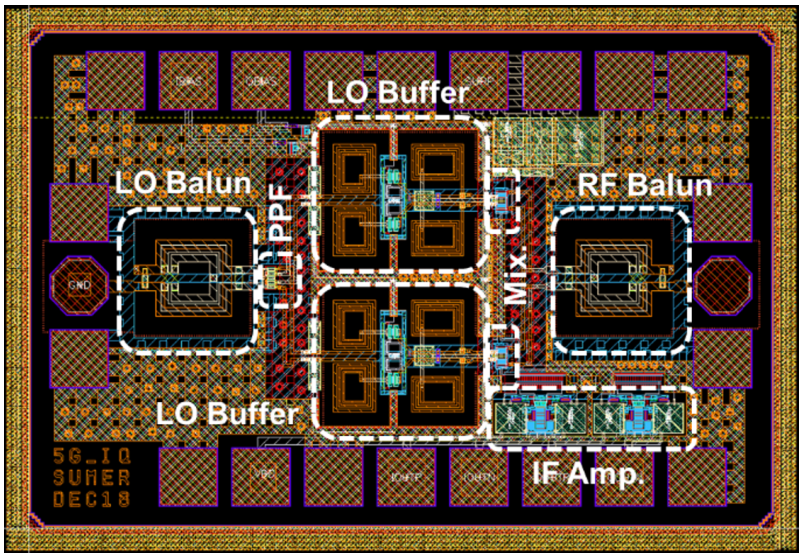


Figure 3.24: Layout view of the 26-GHz, low-power, compact, IQ-downconverter. Die area is 0.7×1.0 mm^2.

buffers, which help mitigate the amplitude balance between the IQ signals and also increase the signal level so that mixers are well driven. Mixers are implemented as NMOS based passive mixers to achieve good linearity and low power consumption. IF signals are amplified by a fully-differential opamp based feedback amplifiers. These differential dc/baseband I and Q signals will be used to track the magnitude and phase of the residual SI signal at the RX output, in order to to update the control voltages of the adaptive SIC network.

The final layout of the IQ downconverter is shown in Fig. 3.24. It is very compact and occupies only 0.7×1.0 mm^2 die area including the pads. Previously designed baluns are used at the inputs, as well as the RC PPF.

3.3.1 LO Buffers

Extremely compact, differential LO buffers are designed using single-stage cascode topology, with an area less than 0.25×0.25 mm^2. Extreme miniaturization is achieved by increasing the number of turns of base and collector inductors, with 3.5 and 3 turns, respectively. The inner turns utilize narrower (2 μm) and outer turns utilize wider (4 μm) metal lines to achieve the same inductance in a much smaller area. The LO buffer, when simulated with a differential 100 Ω input and output port, has a gain of 19 dB at the center frequency of 26 GHz, and draws 18 mA of

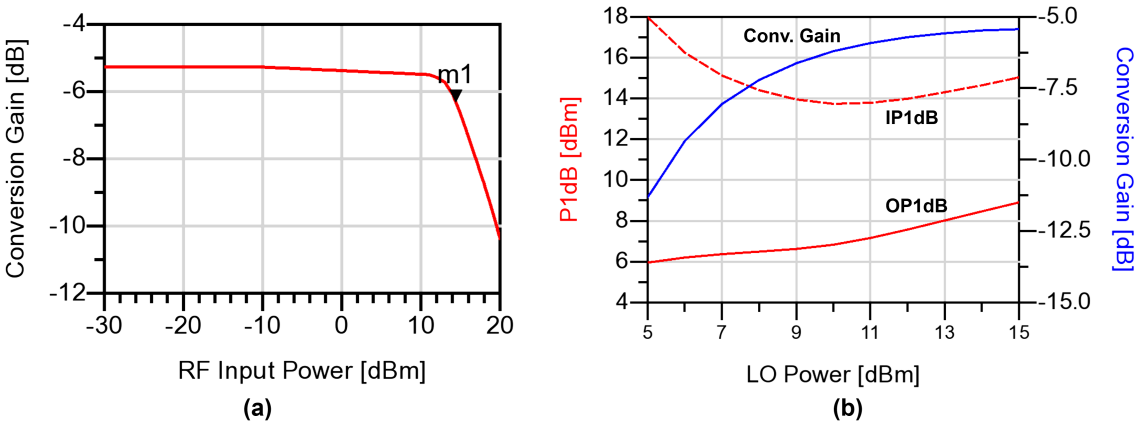


Figure 3.25: Simulated performance of the NMOS passive ring mixer: (a) Conversion gain vs. RF input power. (b) P1dB and conversion gain vs. LO input power.

quiescent current from a 2.5 V supply for a total dc power consumption of 45 mW.

3.3.2 Passive Mixer

A standard passive ring mixer is implemented with 40μm/0.13μm n-channel MOSFET devices that are laid out in a fully symmetric manner. Its simulated performance is shown in Fig. 3.25, in which all ports are terminated with differential 100 Ω impedance. It has a conversion loss of 5.3 dB and IP1dB of 14 dBm for an LO power of 10 dBm. Increasing LO power further improves the linearity, but not the conversion loss.

3.3.3 Baseband Amplifier

Since the RF signal is coupled from the RX path via a capacitive coupler, the incoming RF signal of the downconverter can be modeled with a high Thevenin impedance. This means that the passive mixer in this work operates in *voltage mode*. Therefore, the passive mixer must be followed by a "voltage amplifier" unlike the transimpedance amplifiers that are used after the current mode switching mixers in wideband RF receivers.

With this motivation, a 2-stage opamp shown in Fig. 3.26 was designed. The opamp benefits from the BiCMOS process by incorporating high performance HBT devices as the input differential pair, while the rest of the devices are high-voltage

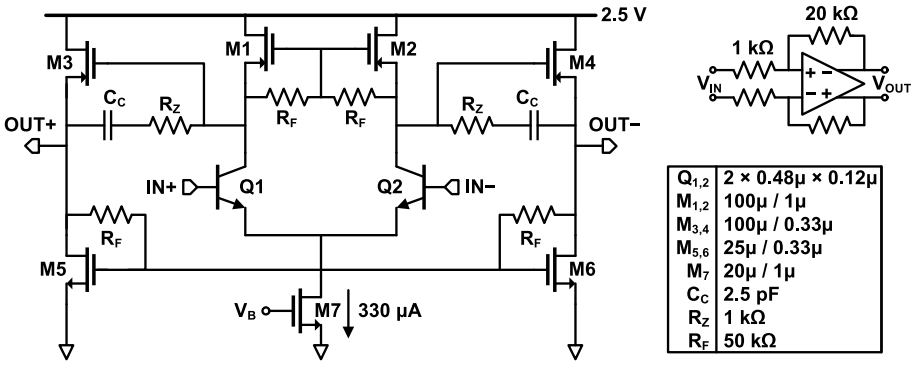
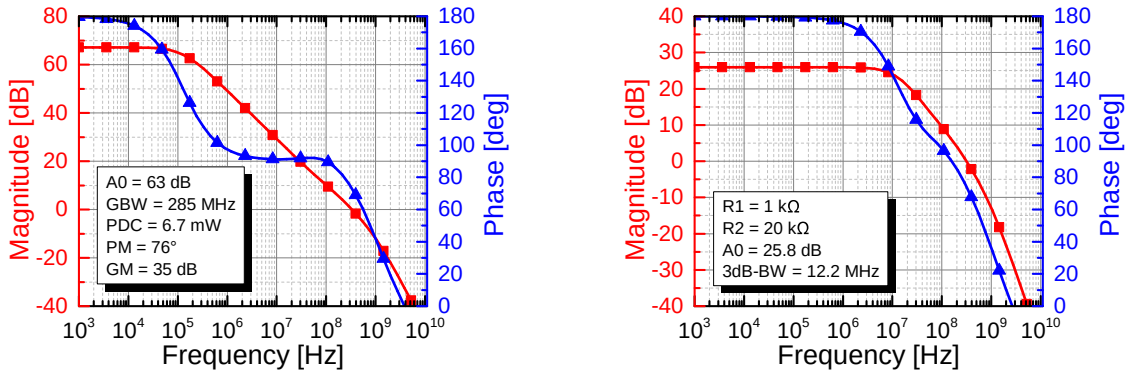


Figure 3.26: Schematic view of the baseband amplifier employing a fully-differential, high-performance, BiCMOS opamp in a negative feedback loop.



(a) **(b)**

Figure 3.27: Simulated (a) open-loop and (b) closed-loop performance of the differential baseband amplifier.

(3.3 V) MOSFETs. Conventional Miller compensation is employed. Large 50 kΩ resistors provide the neccessary common-mode feedback. The opamp was designed to drive a 10 pF load, considering the oscilloscope probes as the ultimate load. Fig. 3.27(a) shows the open loop performance of the opamp. It achieves 63 dB open-loop gain with 285 MHz unity gain frequency using only 6.7 mW dc power consumption. It has sufficient phase and gain margins of 76° and 35 dB. The opamp is used in a fully-differential feedback configuration with 1 and 20 kΩ resistors and the performance is shown in Fig. 3.27(b). The amplifier achieves 26 dB gain with a 3-dB bandwidth of 12.2 MHz, which is sufficient for fast measurement of the residual SI signal power.

3.4 Other RF Building Blocks

This section discusses some of the rest of the RF building blocks of the transceiver shown in Fig. 3.1. For the implementation details of the 3-b attenuator with 1-dB steps realized using the switched-Π topology, see Section 4.1.3 for implementation details. For the details regarding the LNA and PA, see Section 4.1.4.

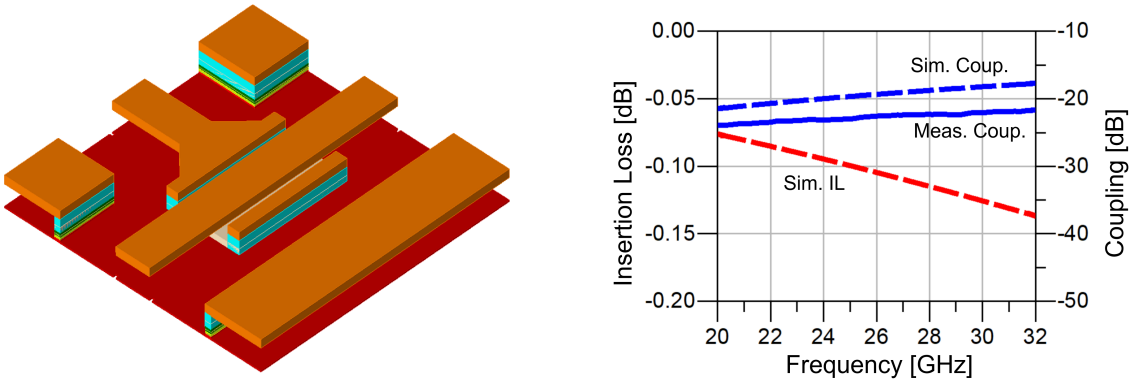
3.4.1 Variable-Gain Amplifier

A cascode HBT based current steering VGA was designed simultaneously for the beamformer ICs and the full-duplex transceiver. VGA enables almost linear-in-dB gain control by using a large, diode-connected HBT, as explained in more detail in Section 4.1.2. However, the control circuitry of the VGA was modified regarding the target SI cancellation specifications of the FD transceiver.

Three blocks are distributively used in the SI canceler for amplitude control: 1) analog-controlled, reflection-type attenuator right after the coupler (~12 dB range), 2) 3-b digitally controlled, switched-Π type attenuator, and 3) the VGA. Evidently, the first one performs the coarse control, the second performs moderate control, and VGA has to perform fine control of the amplitude levels.

From (3.3) and Fig. 3.3, it can be seen that even with infinite phase resolution, a 0.5-dB/step VGA would marginally satisfy the 30-dB SI cancellation requirement. The IQ modulator presented in this chapter has a maximum measured phase step of 0.65°, which necessitates the use of 0.25-dB/step VGAs for reliable 30-dB SI cancellation. We introduce one more additional bit for safety of operation, so that the VGA control must be 6-b with a 0.125-dB/step.

The 6-b VGA control circuitry was implemented using a current-steering DAC similar to Fig. 3.10. The difference is that the three MSBs were implemented as segmented current-steering DAC, while the remainin three LSBs were implemented as binary-weighted current-steering DAC. Unlike the vector modulator case, in which large device sizes are used instead of segmentation to ensure linearity, segmentation is necessary for the VGA, since the output of its current steering DAC is effectively single-ended, i.e. only one branch of the differential outputs of the DAC drives the



(a) **(b)**

Figure 3.28: (a) 3D view of the 20-dB capacitive coupler. (b) Simulated and measured performance.

diode-connected HBT in Fig. 4.4(a).

3.4.2 Capacitive Coupler and Reflective Attenuator

In self-interference cancellation systems, a portion of the transmitted signal is coupled to the canceler network. This is conventionally achieved by directional couplers at low frequencies. In this work we employ a capacitive coupler due to its very compact size. Its implementation is shown in Fig. 3.28(a). Between the PA output and the TX_{OUT} pad, a custom designed MOM cap is introduced below and around the signal line of the CPWG transmission line. The geometry was optimized to achieve an em-simulated coupling value of 20 dB. The insertion loss penalty in the TX path is only 0.1 dB.

The signal coupled by the capacitive coupler is further attenuated in the FD transceiver by a reflective attenuator in the form of a shunt NMOS device with the size of $2 \times 40\mu m/0.13\mu m$, whose gate terminal is connected to a control via a large resistor. A breakout of the coupler + attenuator cascade was fabricated and tested. The measured coupling value in the reference mode of the attenuator is 3 to 4 dB lower compared to the em simulations. Similarly, the attenuation control range was designed to be 16 dB in simulations, which turned out to be 3 to 4 dB lower. These results suggest that the deviation in the coupling value in Fig. 3.28(b) is mainly caused by the reflective attenuator and that the capacitive coupler performance is in agreement with em simulations.

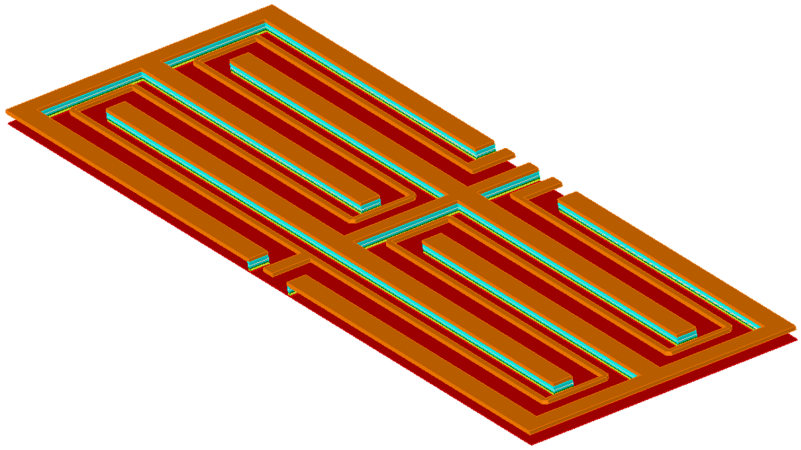


Figure 3.29: 3D layout view of the conventional Wilkinson combiner/divider implemented using TM2 and M3 layers.

3.4.3 Wilkinson Combiner

A conventional Wilkinson combiner was designed using a TM2-M3 CPWG transmission line. Using a meandered strucute as in Fig. 3.29 the overall area was minimized. It has an em simulated 1 dB insertion loss, which was also verified through measurements. The total die area is $0.225 \times 0.7 = 0.16$ mm^2. This wilkinson was employed in the four-element beamformer ICs presented in the next chapter. For area considerations, a lumped-element wilkinson was designed for the full-duplex transceiver.

3.4.4 Switchable Wilkinson Combiner

The concept of a switchable/configurable wilkinson divider was motivated by two factors. First was the large die area occupied by the conventional wilkinson. A more important factor was the fact that main TX leakage through the duplexer or the shared antenna interface is slowly changing in time. Therefore, once the optimum phase/amplitude control settings of the canceler has been found, the switchable wilkinson can be configured in TX only mode, in order to avoid the TX insertion loss penalty due to the wilkinson.

With these incentives, the lumped-element wilkinson shown in Fig. 3.30(b) was designed. Series/shunt isolated NMOS switches are introduced to the third port of the wilkinson as seen in Fig. 3.30(a). When M_1 is OFF and M_2 is ON, it operates

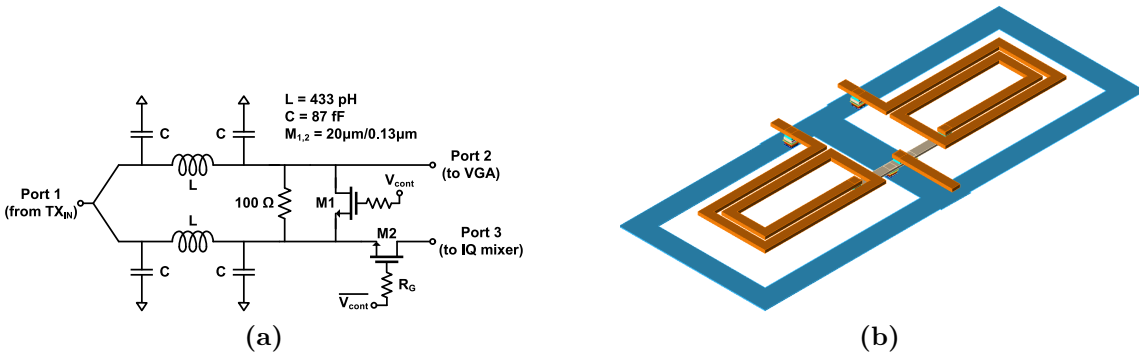


Figure 3.30: (a) Schematic view of the switchable lumped-element Wilkinson divider. (b) 3D view of the lumped-element Wilkinson.

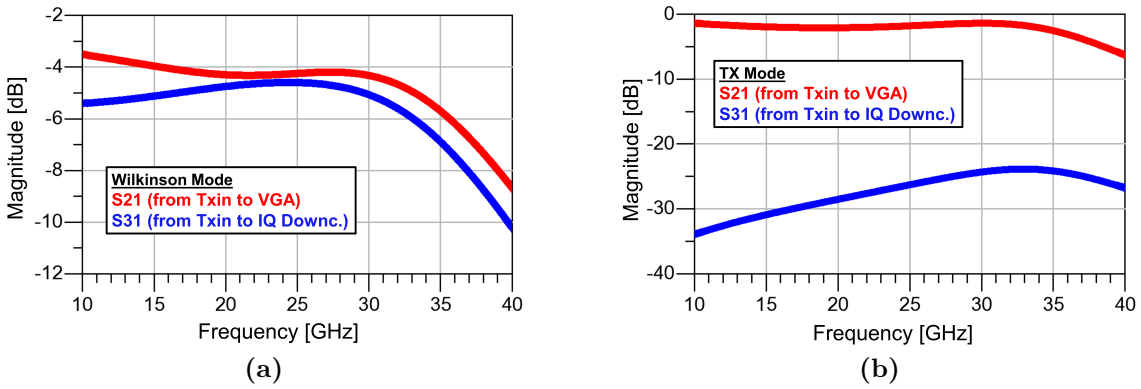


Figure 3.31: EM simulated performance of the switchable Wilkison divider: (a) Calibration mode (equal division) and (b) TX-only mode.

in normal/conventional wilkinson divider mode. In this case, as can be seen in Fig. 3.31(a), the TX insertion loss is about 4.1 dB and the insertion loss to the IQ downconverter is 4.7 dB, the asymmetry caused by the ON resistance of M_2. When M_2 is OFF and M_1 is ON, both branches of the wilkinson is effectively connected to Port 2. An ideal wilkinson divider having it two outputs combined together into a single port is no longer matched at its input. But it can be derived as

$$S_{11} = \left(-\frac{j}{\sqrt{2}}\right)^2 \left(-\frac{1}{3}\right) = \frac{1}{12}, \tag{3.9}$$

which equals to an input return loss of 21.5 dB, neglecting the effect of the ON resistance of M_1. In this mode, the simulated TX insertion loss is only 1.5 dB, as seen in Fig. 3.31(b).

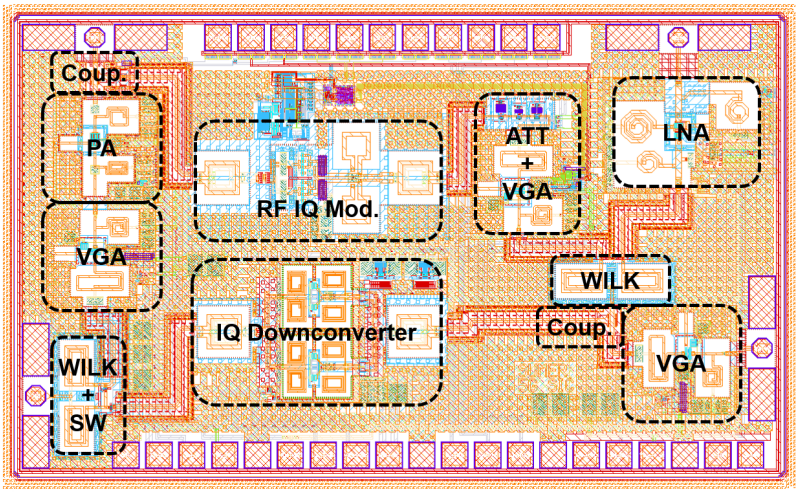


Figure 3.32: Layout of the fabricated full-duplex transceiver with on-chip analog/RF self-interference canceler and a low-power IQ downconverter. Die are is $2.35 \times 1.41 = 3.31$ mm^2.

3.4.5 Complete Full-Duplex Transceiver

The complete full-duplex capable transceiver with self-interference cancellation capabilities has been developed, and the final layout is shown in Fig. 3.32. The IC occupies $2.35 \times 1.41 = 3.31$ mm^2 die area and has the following features.

- A switchable Wilkinson combiner/divider that can operate either in calibration mode (equal division to TX an IQ downconverter) or TX only mode.
- A high-performance I/Q vector modulating phase shifter with 10-b monotonic phase control
- A 6-b VGA with 0.125-dB steps, based on segmented 3-b operation and current-steering topology
- A 3-b switched Π-type attenuator with 1-dB steps
- A 20-dB capacitive coupler at the TX output followed by a reflective attenuator with ~12 dB range
- A relatively high-efficiency class-AB power amplifier with 30% PAE at an OP1dB of 12 dBm
- A high linearity LNA (10 dBm OP1dB)

Chapter 4

26-GHz Four-Element Transmitter and Receiver RF Beamformers in 130-nm SiGe

This chapter presents 26-GHz transmit and receive channels of a four-element phased array beamformer integrated circuit realized in a 0.13-μm SiGe BiCMOS technology. Fig. 4.1 shows a four-element analog/RF beamforming architecture for phased array systems. Both RX and TX channels in this thesis was designed according to the 5G band in 24.25–27.5 GHz. Single-channel RX and TX ICs are suitable for massive-MIMO applications and do not incorporate the step attenuators. The four-channel RX and TX versions do include the step attenuators. The ICs provide 6-b phase control and 3-/4-b amplitude control for single-channel / four-channel beamformers, respectively.

4.1 Building Blocks

Each RX channel consists of an LNA, PS, and VGA. Among the three building blocks, PS exhibits the largest NF, either due to its passive topology, or due to employing passive structures such as a balun and I/Q generator in the case of vector modulator topology. Placing the PS at the end of the channel to achieve the best NF

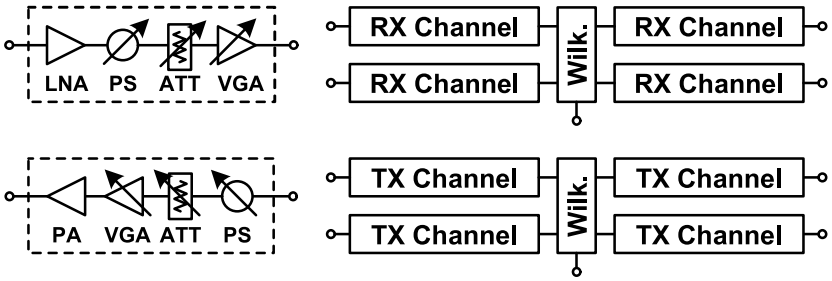


Figure 4.1: Block level view of single-channel (left) and four-channel (right) analog beamforming receiver and transmitter front-ends.

is not ideal, since the channel linearity will be severely limited. Hence, the PS was placed after the LNA to achieve moderate (> -30 dBm) IP1dB levels. To achieve the challenging NF spec (< 3.5 dB), a noise cancellation technique was employed in the LNA. Further, a low-loss lumped-quadrature hybrid was preferred for I/Q generation in the PS, instead of a conventional RC polyphase filter that would be more compact but more lossy.

Channel gain should be maximized within the limits of linearity specifications to suppress losses and noise contributions of the following blocks. However, when many such channels are combined in a single die, the total channel gain and LNA gain should be kept below 30 and 15 dB, respectively. Excessively high channel gain poses potential stability problems; and excessively high LNA gain causes beam steering errors due to crosstalk between adjacent channels. sed.

4.1.1 Phase Shifter

Many works can be found in the recent literature focusing on mm-wave 5G phase shifters employing various topologies such as vector modulation [94–96], switched-LC [97, 98], tunable transmission line [99], and reflective-type phase shifter (RTPS) [100].

The PS in this work is based on the I/Q vector modulator presented in the previous chapter (see Fig. 4.2). However, some modifications are required for its use in a phased array channel. The 2-stage RC polyphase filter is quite lossy and it is not feasible to use it in phased array RX channels. Therefore in this PS, in-phase and quadrature signals are generated using two lumped quadrature hybrid couplers,

as shown in Fig. 4.2(c). Overlapping, single turn, 4-μm wide TM2 and 8-μm wide TM1 layers are used as the primary and secondary coils. With a diameter of 160 m, they exhibit an inductance of 400 pH and a magnetic coupling coefficient of k = 0.71. The shunt capacitors required for the coupler are embedded into the coil parasitics. Since this IQ generation scheme is pseudo-differential (two separate couplers are used) unlike RC polyphase filters, it does not provide common-mode suppression.

This leads us to the second modification. The amplitude imbalance of the transformer balun discussed in Section 3.2.1 is high at 0.35 dB. That was not an issue since it was followed by a 2-stage RC polyphase filter, which provide sufficient common-mode rejection. Due to the pseudo differential operation of lumped-quadrature hybrids in the modified version, the amplitude imbalance of the balun becomes a bottleneck and must be taken care of.

With this motivation another transformer balun was designed, as can be seen in Fig. 4.2(b) and Fig. 4.3(a). It employs a single-turn secondary coil, which improves the overall symmetry of the balun (the only asymmetry coming from the ground connection of the primary and the center tap of the secondary), therefore reducing the amplitude imbalance. The primary and secondary coils have a self-inductance of 225 abd 235 pH, respectively, with a coupling coefficient of 0.62. The transformer balun has an em simulated insertion loss 1.5 dB at 26 GHz, with an amplitude and phase imbalance of 0.2 dB and 1°.

Compared to the previous balun reported in Section 3.2.1, this transformer balun has a better amplitude imbalance but a worse phase imbalance. The slightly degraded phase imbalance is not an issue though for two reasons: First, the IQ generator employs a tuning knob to mitigate the effect of balun amplitude/phase imbalances. Second, the beamformer channel will have 5- or 6-b phase control, in which case $\pm 1^\circ$ phase imbalance of the balun would not matter. And finally, the actual phase imbalance will probably be much higher due to process variations anyway.

The third modification, as mentioned in the previous paragraph, is that we introduced a tunable resistive termination at the isolated port of the coupler to compensate for possible IQ amplitude/phase imbalances that may be caused either

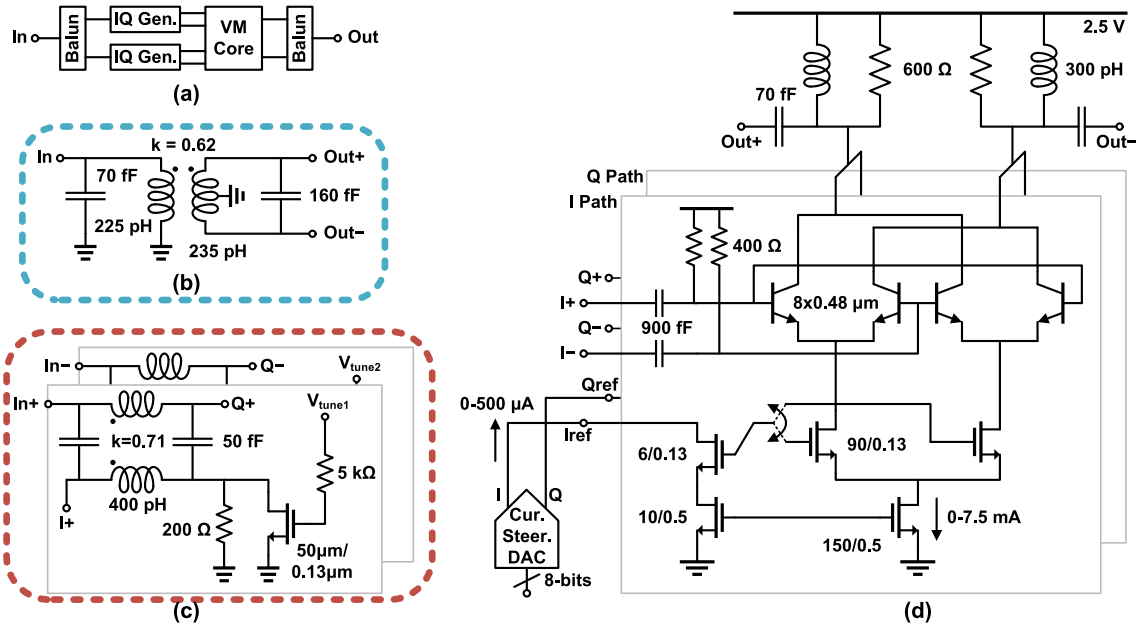
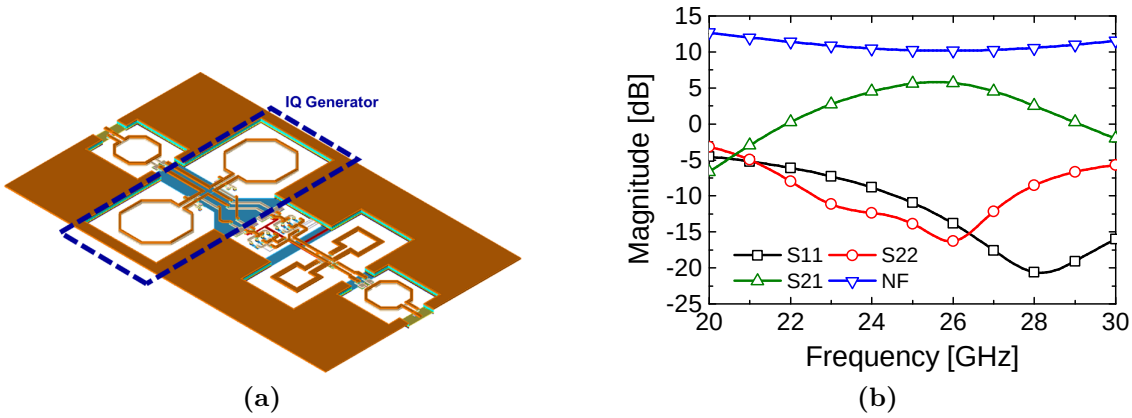


Figure 4.2: (a) Overall phase shifter system and schematic views of (b) tuned transformer balun used at the input and output of the PS, (c) lumped quadrature hybrids used to generate I/Q signals, and (d) phase shifter with Gilbert-cell type vector-modulator.

by the balun or the IQ generator itself. The isolated port of the coupler is terminated with a 200-Ω resistor in parallel with an NMOS device (see Fig. 4.2(c)). As the NMOS threshold voltage of the process is 0.4 V, applying a control voltage in 0.5–1 V range changes the effective termination resistance in 20–80 Ω range. This mismatch introduced to the isolated port is adequate to tune out any phase imbalance caused by either the balun or the pseudo-differential IQ generator itself.

A 3D em simulated view of the overall phase shifter is shown in Fig. 4.3(a). The overall area of the phase shifter is 0.6×1 mm^2 and the size of the lumped quadrature hybrid based IQ generator is 0.3×0.6 mm^2. The overall PS has an EM-simulated gain of 5.5 dB at 26 GHz and draws a total of 7.5 mA current from a 2.5 V supply. A benefit of this vector modulator topology is that power consumption does not change between different phase states. The simulated noise figure is 10 dB at 26 GHz.



(a) (b)

Figure 4.3: (a) 3D layout view of the modified vector modulator phase shifter employing lumped quadrature hybrids for IQ signal generation. (b) Simulated performance of the PS.

4.1.2 Variable Gain Amplifier

Phased-array beamformer channels employ attenuators or variable-gain amplifiers (VGAs). Their primary objective is to apply some amplitude window function on the array level, i.e. amplitude tapering, to reduce array sidelobe levels and to control sidelobe null directions for spatial interference rejection. They can also be used to compensate for phase shifter gain variation across its different phase settings. Many works in the literature has focused on variable-gain amplifiers for 5G beamforming applications [101–105].

In this work we use a single-stage, cascode amplifier with current-steering as the VGA. Its schematic is shown in Fig. 4.4(a). The CE and CB transistors are sized eight times the unit device, to achieve a good trade-off between gain and linearity. The emitter terminal of a larger (32×unit device), diode-connected HBT is connected to the intermediate node of the cascode stage, and its other terminal is connected to a control voltage via a 500 Ω resistance. This design allows almost linear-in-dB amplitude control up to a ~10 dB range, when the control voltage is linearly swept with 100-mV steps.

The em-simulated performance of the VGA is given in Fig. 4.4(b). It has a peak gain of 17 dB and a gain control range of ~8 dB while drawing 4.7 mA from a 2.5 V supply. At the center frequency of 26 GHz, the VGA has a phase variation of ±5°. It has an IP1dB of −16 dBm, with a dc power consumption of 13 mW. The VGA

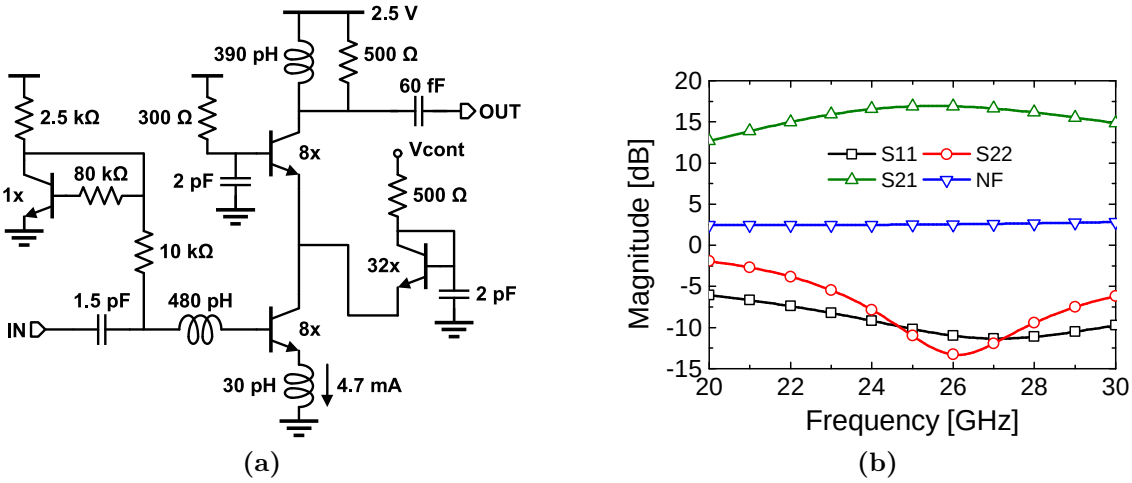


Figure 4.4: (a) Schematic view of the VGA with linear-in-dB gain control and (b) its simulated small-signal performance at the reference state.

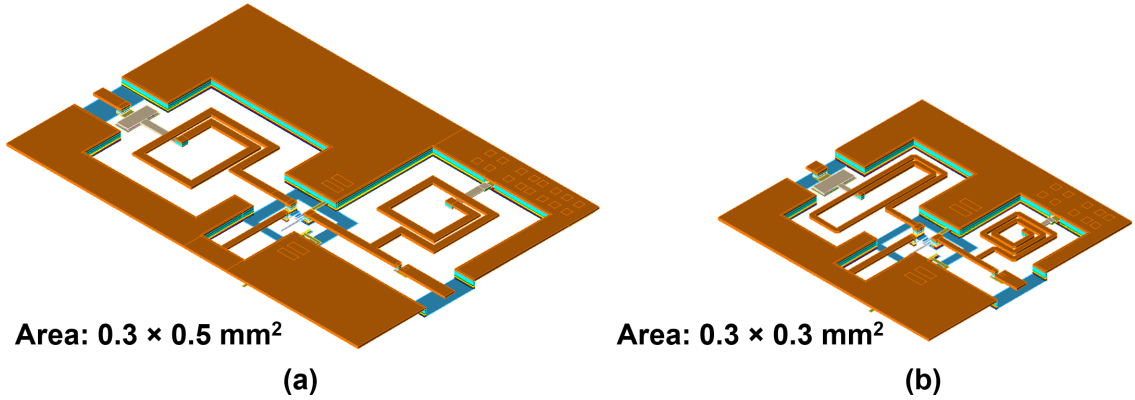


Figure 4.5: (a) The initial layout design of the VGA that was used in the single-channel RX and TX beamformers. (b) Miniaturized form of the VGA that was used in the four-channel beamforming ICs.

include its own active biasing circuitry and utilize a shunt output resistor to widen its output matching bandwidth.

Fig. 4.5 shows two different layout versions of the same VGA schematic. The first version shown on the left was slightly larger and was used in the single-channel beamformers. The second version shown on the right is a miniaturized version of the other. Miniaturization is achieved by 1) elongating the base inductor perpendicular to the signal line, 2) increasing the number of turns of the collector inductor, and 3) decreasing the metal widths of both inductors. The penalty here is the slight reduction in their quality factors, which was not an issue for the overall beamformers in terms of noise figure and gain.

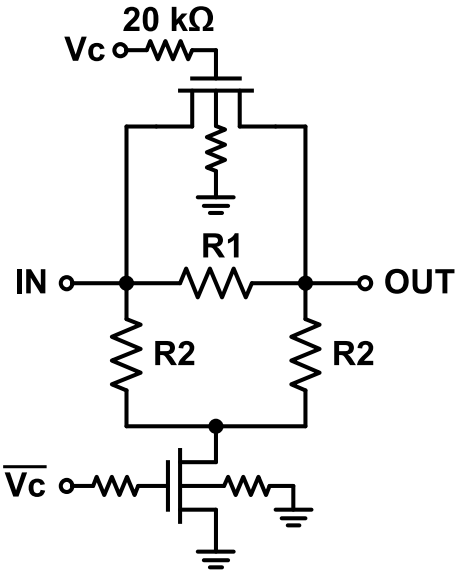


Figure 4.6: Schematic view of a Π-type attenuator with gate/body floated, isolated NMOS transistors.

4.1.3 Step Attenuator

Although not used in the single-channel RX/TX beamfomers, digitally controlled step attenuators are used in the four-channel beamformers, as well as the self-interference cancelling circuitry presented in the previous section. In this work, a 3-b digitally-controlled attenuator with 1-dB steps is designed so that when combined with the 3-b VGA, we achieve effectively 4-b amplitude control with 1-dB steps. A Π-type attenuator stage shown in Fig. 4.6 is used for all the bits, i.e. 1-dB, 2-dB, and 4-dB. All the stages uses the same series and shunt isolated NMOS transistors with sizes 40μm/0.13μm and 20μm/0.13μm, respectively.

With ideal switches, a Π-type attenuator can achieve a desired attenuation between ON and OFF states, while maintaining perfect matching for both modes of operation, without any phase variation between the modes of operation. However, due to the non-ideal ON-resistance and OFF-capacitance of the switch, some performance have to be sacrificed. This is especially valid for non-SOI silicon processes that are not optimized for high frequency switching applications.

For given transistor sizes (which have to be optimized on their own), there are infinitely many resistor value pairs that provide a desired attenuation between ON and OFF states. One of those pairs minimizes the return loss variation and another

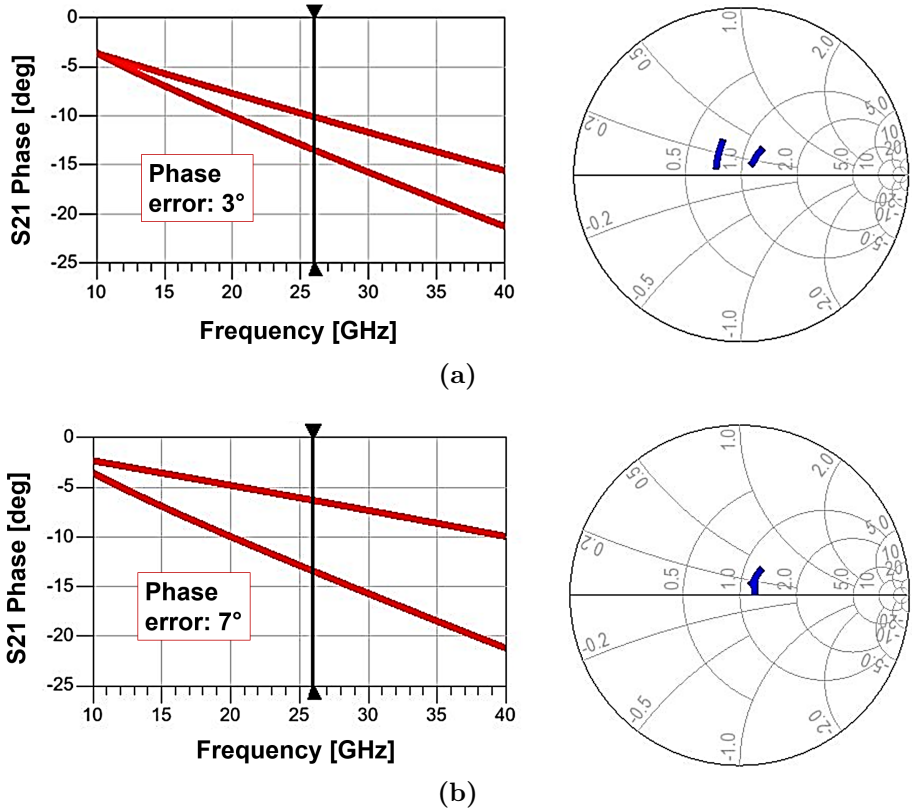


Figure 4.7: Comparison of two different design methdologies for Π-type attenuators with nonideal switches: (a) Minimum phase error between ON/OFF states, and (b) Minimum reflection coefficient deviation between ON/OFF states.

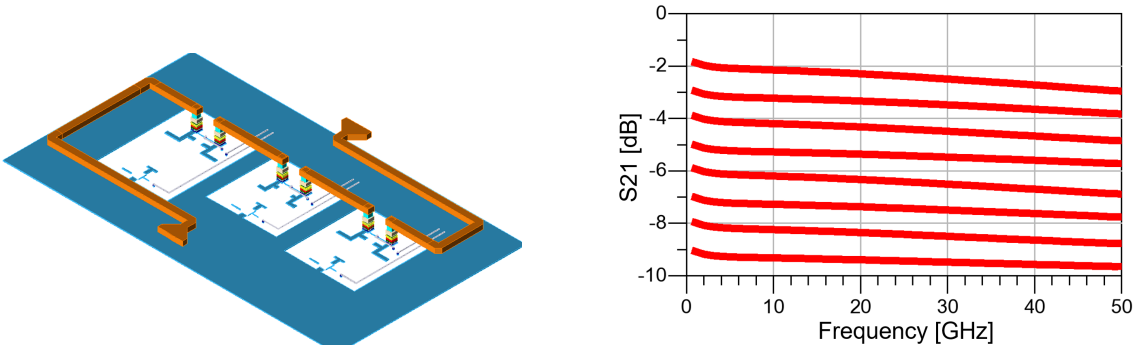
pair minimizes the phase variation between the two modes of operation.

Let's exemplify this trade-off using an 8-dB switched Π-type attenuator. We do not use this attenuator in our systems, we just use this to make a demonstration. Using the same transistor sizes as mentioned above, and using $R_1 = 50\Omega$ and $R_2 = 42\Omega$ results in 8-dB attenuation. The phase and return loss variation of this implementation is shown in Fig. 4.7(a). This is the resistor pair that provides the minimum phase variation (~3°), however the reflection coefficient (or input impedance) greatly alters between the ON/OFF states. The normalized input impedance is around $0.8 + j0.2$ and $1.2 + j0.2$ for the ON and OFF states, respectively.

On the other hand, using $R_1 = 80\Omega$ and $R_2 = 95\Omega$ Ω with the same transistor sizes again results in 8-dB attenuation. The phase and reflection coefficient variation is shown in Fig. 4.7(b). Note that the phase variation is greater (~7°), but the reflection coefficient is almost the same between different modes of operation.

Table 4.1: Resistor component values fothe 3-b Π-type attenuator.

Stage	R_1 [Ω]	R_2 [Ω]
1-dB	10	760
2-dB	18	430
4-dB	35	220



(a) **(b)**

Figure 4.8: (a) 3D layout view of the 3-b Π-type attenuator and (b) simulated S21 across its different settings.

We decided to design the attenuator using the latter methodology, because it offers improved reliability. The reason is that, when two or more attenuator bits are cascaded, they load the preceding and following stages according to their input/output impedances. If the input/output reflection coefficient of an attenuator stage does not stay the same between its ON/OFF states, then the loading on the preceding/following stages is changed, causing an error in the attenuation level, which is strongly undesired. The only downside of the methodology is the increased phase variation, which turns out to be ±3°. This is acceptable considering the phase shifter resolution in the array is 6-b, i.e. 5.6° steps.

Table 4.1 shows the resistor values for the complete 3-b attenuator design. Its final layout is shown in Fig. 4.8(a). The total area is 0.12×0.22 mm^2. The long TM2 lines at the beginning and end are approximately 50 pH inductors, which help match the input/output impedance by neutralizing the OFF-capacitance of the series NMOS switches. The simulation results are given in Fig. 4.8(b) and Fig. 4.9. The attenuator has and insertion loss between 2-9 dB with a practically zero rms amplitude error at 26 GHz. You can see that that return losses change negligibly

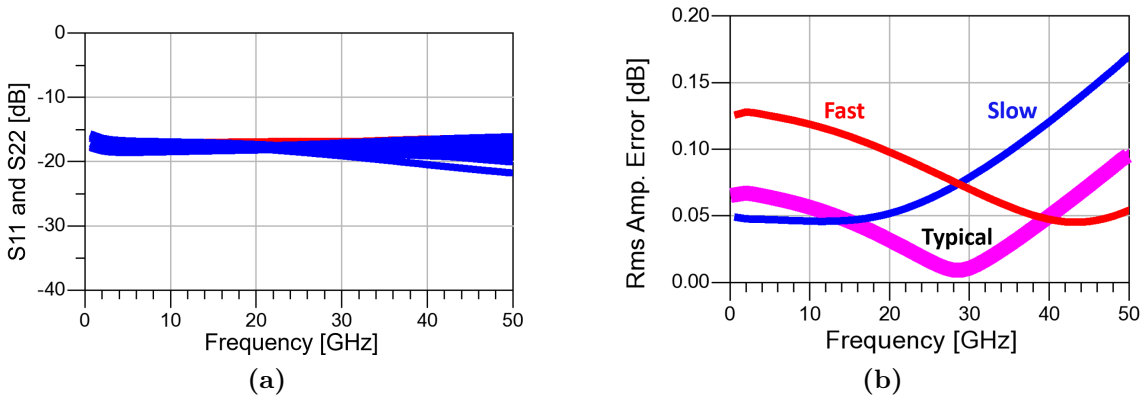


Figure 4.9: (a) Simulated return loss of the 3-b attenuator for different attnuation settings. (b) Simulated rms amplitude error vs. process corners.

across different attenuation settings. The phase variation across attenuator settings is $\pm 3^{\circ}$. The design method is tested against process corners (Fig. 4.9(b)) and the results show less 0.1 dB error within the desired band of operation.

4.1.4 Low-Noise and Power Amplifiers

The low noise amplifier was designed by my colleague Abdurrahman Burak. It is based on a cascode topology and employs several unconventional design techniques. First, it utilizes a shunt base inductor to avoid the parasitic resistance of a series base inductor that limits the achievable NF [106]. Second, HBTs are sized slightly larger than required for the optimum source resistance ($R_{S,\text{opt}}$) to be 50 Ω. This improves the linearity without significantly affecting NF, as the equivalent noise resistance (r_n) of the process is very low. Finally, a noise reduction technique is employed by placing a shunt inductor to the intermediate node of the cascode [107]. This resonates out the parasitic capacitance at that node, which—if left unchecked—increases the noise contribution of the CB transistor at high frequencies. The reason is that the noise current injected to that node would be divided between the parasitic capacitance and the impedance looking into the emitter ($1/g_m$). A standalone version of the LNA was fabricated and measured. The measured gain and NF is 11 and 2.5 dB at 26 GHz. The LNA draws 5 mA current from a 3.2 V supply.

There are many works in the literature that focus on high-efficiency, high-power PAs for integrated 5G phased-arrays in SiGe [108–110] and CMOS [111–114], as well

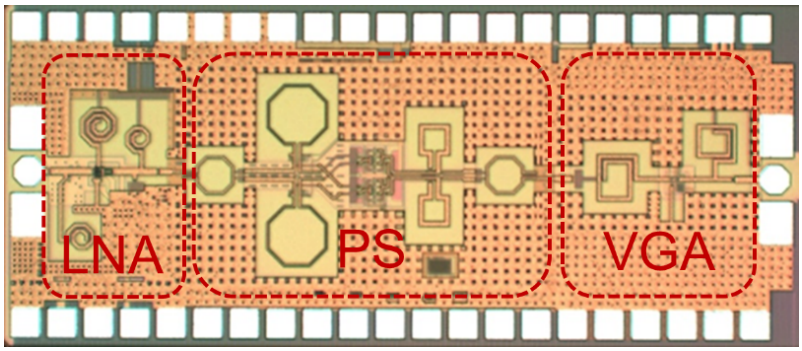


Figure 4.10: Die photo of the RX channel. Die area is 1.33 (1.9×0.7) mm^2 excluding the pads and 1.89 (2.1×0.9) mm^2 including the pads.

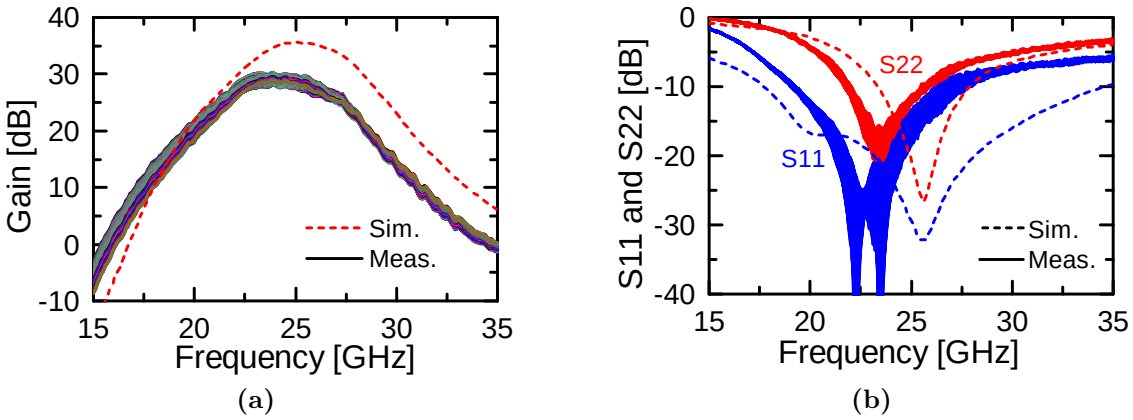
as Doherty [115–117], outphasing [118, 119], and power combining [120] type power amplifiers. The power amplifier in this work was designed by my colleague Alper Guner. It is a 2-stage class-AB amplifier based on cascode topology, operating from a 3.2 V supply. It has a simulated gain of 24 dB, OP1dB of 15 dBm, and power consumption of 140 mW, which increases up to 185 mW when operating at P1dB.

4.1.5 Measurement Results

4.1.5.1 Single RX Channel

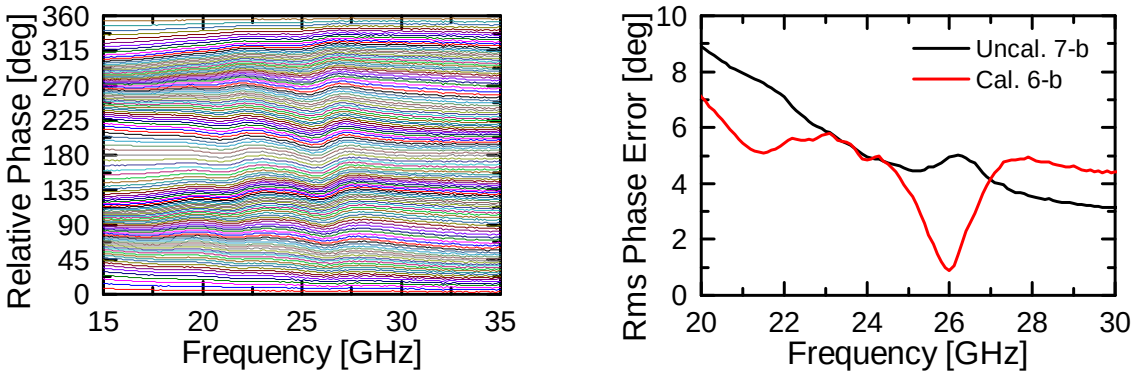
The RX channel was fabricated in IHP SG13S BiCMOS technology (see Appendix A for process details). The chip micrograph is shown in Fig. 4.10. The chip area is 1.33 mm^2 excluding the pads and 1.89 mm^2 including the pads. The measurement setup is similar to the one shown in Fig. 3.17. 100-µm Infinity probes were used for RF input/output and 24-pin GGB probes were used for dc supply and bias voltages. The digital control signals were given by a Spartan 3E FPGA.

S-parameters were measured with a Rohde & Schwarz ZVA67 network analyzer after performing SOLT calibration up to the probe tips using an impedance standard substrate (ISS 101-190). The measured gains for all the phase states are shown in Fig. 4.11(a). The average gain peaks at 24 GHz with a value of 28.5 dB and its 3-dB bandwidth is between 22 and 27 GHz. Although there is a ~7 dB difference between simulated and measured values, the overall behavior is the same except a slight shift (~2 GHz) to lower frequencies. A similar behavior was observed in the LNA breakout measurements. These results suggest that there is a 2-3 dB difference between the



(a) (b)

Figure 4.11: Simulated and measured (a) gain and (b) input/output reflection coefficients across all phase states.



(a) (b)

Figure 4.12: (a) Measured relative phase shifts for 7-b phase control. (b) Uncalibrated 7-b and calibrated 6-b rms phase errors.

simulated and actual gain of each sub-block. This discrepancy is mainly related with active device modelling and partly related with EM modeling of degeneration inductors. The gain variation across different phase states was measured to be ±1.5 dB. Measured input and output return losses are shown in Fig. 4.11(b) and they do not vary significantly for different phase states. $S_{11} < -10$ dB in 19–27 GHz and $S_{22} < -10$ dB in 22–26 GHz.

Fig. 4.12(a) shows the relative phase shifts of the RX channel. Only 7-b data is plotted for visual clarity. All the $2^{10} - 4$ phase states were inspected, and a completely monotonic behavior was observed, that is free of any overlaps or dead zones. These raw results were obtained without any type of phase calibration. Fig. 4.12(b) shows that the rms phase error for the uncalibrated 7-b control is around

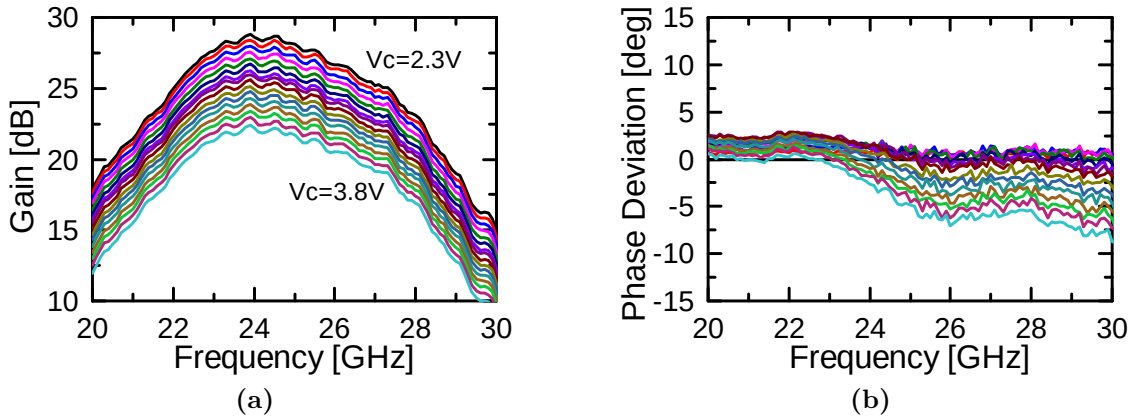
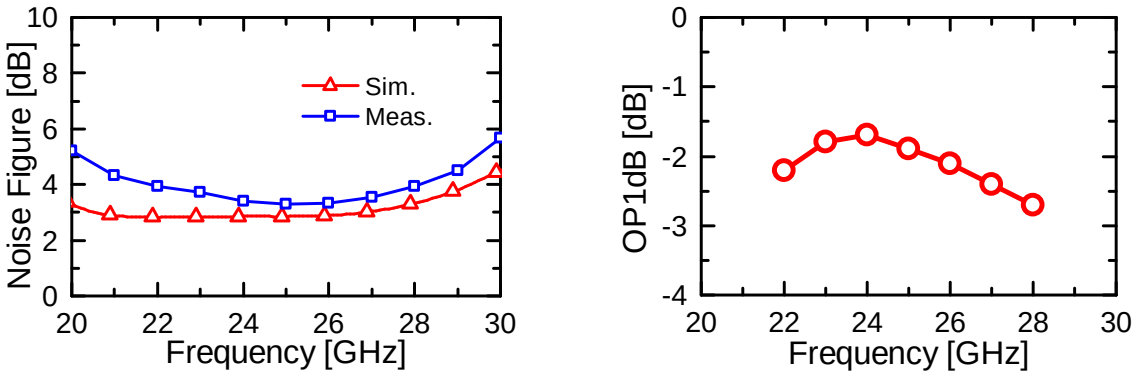


Figure 4.13: (a) Measured 6-dB gain control with 0.4-dB steps. V_C is swept from 2.3V to 3.8V with 100mV steps. (b) Phase deviation across different amplitude settings.

4-5 dB in 22–27 GHz band. The same figure also shows that the rms phase error is reduced to 0.2° when calibrated for 6-b operation at 26 GHz. Rms phase error can be reduced to almost zero at any center frequency, as the phase shift vs. frequency behavior is flat. The slight upward slope around 26 GHz is caused by the high-pass branches of the lumped-quadrature hybrids.

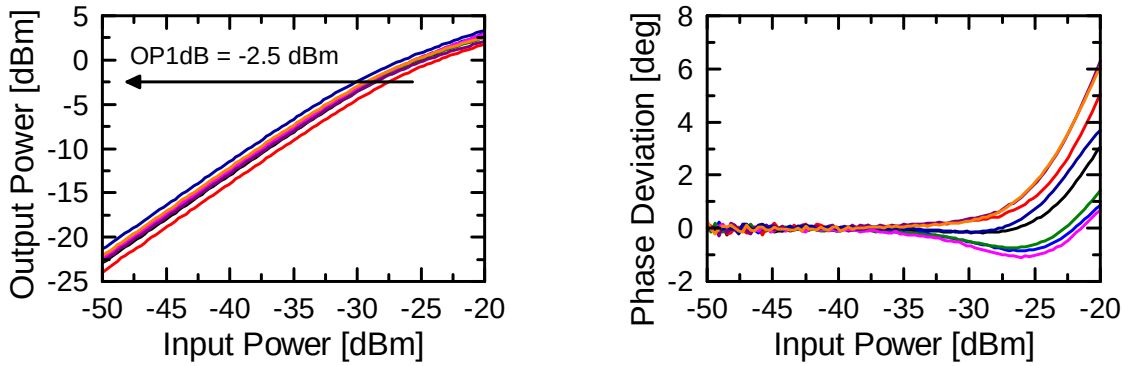
Gain control functionality was verified by measurements and the results are shown in Fig. 4.13(a). VGA control voltage was linearly swept from 2.3 V to 3.8 V with 100 mV steps. The results show linear-in-dB control in a 6-dB range. Within the 3-dB bandwidth, the phase deviation across different gain settings are less than ±3° for most gain settings (Fig. 4.13(b)). As expected, the worst-case phase deviation occurs for the lowest gain setting, i.e. as more current is steered away from the main cascode stage, and it is around 7°.

The noise figure of the IC was measured with a Keysight E4448A PSA spectrum analyzer and 346CK01 noise source. The cable after the DUT was included in the calibration step. Losses of the cable before the DUT and the RF probes were compensated by measuring their s-parameters and loading the data to the PSA. The measured NF of the RX channel is shown in Fig. 4.14(a). Its minimum value is 3.3 dB, and it is better than 4 dB within the 3-dB bandwidth of 22–27 GHz. The simulated NF is also shown in Fig. 4.14(a), which includes the measured data for the LNA and simulated data for the rest. The discrepancy between simulated and



(a) (b)

Figure 4.14: (a) Simulated and measured noise figure of the RX channel. (b) Measured OP1dB at different frequencies.



(a) (b)

Figure 4.15: (a) Measured output power vs. input power for eight major phase states at 26 GHz. (b) Masured phase deviation vs. input power.

measured NF is around 0.3 dB at the center frequency.

For NF measurements, PSA was operated at zero span to reduce the uncertainty, i.e. NF was measured at frequencies from 20 to 30 GHz with 1 GHz steps at a time. The overall NF uncertainty in this case is limited by the noise source ENR and mismatch uncertainty, and it is calculated to be ±0.3 dB.

The linearity of the RX channel was characterized with a single tone test at several frequencies and eight major phase states using the ZVA67 network analyzer. Source power calibration is performed with a Keysight E4417A power meter and 8487D power sensor. Thru connection of the RF GSG probes were used for receiver power calibration. The measured results are shown in Fig. 4.15(a). Depending on the phase state, at 26 GHz the RX channel achieves −2 to −2.7 dBm OP1dB, which

Table 4.2: Comparison of State-of-The-Art Silicon-Based Phased-Array Receiver Channels at 26 GHz.

Ref.	**This Work**	[22]	[32]	[29]	[26]#	[33]
Process	130nm SiGe	45nm SOI	130nm SiGe	180nm SiGe	28nm CMOS	65nm CMOS
3-dB BW [GHz]	22–27	26–28	27–28.5	28–32	25.8–28	26–30
Phase Res. [°]	5.6	11.2	4.9	5.6	22.5	11.2
Amp. Cont. [dB]	6	6	8	14	12	0
Gain [dB]	28.5	12.2	30	20†	13.5	9.5
NF [dB]	3.3	4	6*	4.6	6.2#	5.5
OP1dB [dBm]	−2.5	3	6.5	−3	−11.5	−13.5
Pdc [mW]	48	42	103	130	50	10
Area [mm^2]	1.33	1.75	2.6*	1.2‡	0.5	0.32

* Estimated from the micrograph of the 32-element TRX IC. Reported NF includes TRX switch loss.

† Includes the ohmic losses of the on-chip 4-way Wilkinson combiner.

‡ Estimated from the micrograph of the 4-element TRX IC.

Includes only LNA and PS, since VGA is used after combining four channels. Area is estimated from the micrograph. Reported NF includes TRX switch loss.

corresponds to −30 to −28 dBm IP1dB. Fig. 4.15(b) shows the phase deviation vs input power level at the same frequency. It can be seen that operating at P1dB causes only ±1° phase error, which is sufficiently low for accurate beam steering [34]. Finally, Fig. 4.14(b) shows the OP1dB for the reference phase state at different frequencies. Within the 3-dB bandwidth, OP1dB is nearly constant at −2 dBm. The total power consumption of the RX channel is 48 mW and it does not increase noticeably while operating at P1dB.

Table 4.2 compares state-of-the-art silicon-based phased-array receiver channels for 26/28 GHz 5G communications. The presented RX channel achieves the lowest NF of 3.3 dB among the compared works, which can be attributed to factors such as employing a noise reduction technique in the LNA, using a low-loss lumped quadrature hybrid in the PS, the availability of low-noise, high-performance HBTs in IHP SG13S process, and the overall channel design. For fair comparison, it must be noted that references [22,33] are receivers and references [26,29,32] are transceivers. Hence, the latter suffer from NF degradation due to T/R switching. However, it

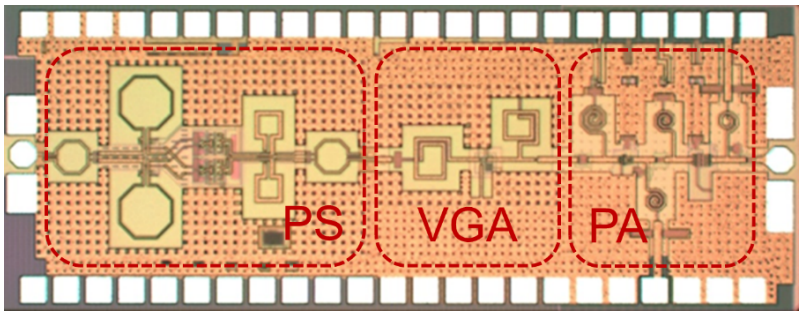


Figure 4.16: Die photo of the TX channel. Die area is 1.5 (2.2×0.7) mm^2 excluding the pads.

was reported that the T/R switch in [32] degrades RX NF by 0.6 dB; so the RX NF of that work becomes 5.4 dB. The T/R switch loss was not reported in [26], but its RX NF still remains higher compared to this work assuming a typical SPDT loss of 2 dB. Finally, even though [29] is a transceiver, the reported NF in Table I is of its RX channel only.

In addition to best NF performance, the presented work also achieves the widest 3-dB bandwidth and the highest bit resolution. Although in this dissertation the phase plots were provided for calibrated 6-b operation (Fig. 4.12) for better visibility, the maximum phase shift between any adjacent phase state is less than 1° , implying that the RX channel can be calibrated for up to 9-b phase control resolution. The presented work also exhibits a high channel gain at 28.5 dB and only [32] is higher. However, that work consumes 103 mW dc power, which is more than twice of the presented work.

4.1.5.2 Single TX Channel

The transmit channel consists of the cascaded phase shifter, VGA and PA, in that order. All the sub-blocks were designed for a 50 Ω input and output termination. They employ a grounded coplanar microstrip interface using a 16-m wide TM2 as the signal layer and M1 as the ground plane. The total TX channel layout is shown in Fig. 4.16 and it occupies 0.7×2.2 mm^2 chip area excluding the pads. The total TX channel has a simulated maximum gain of 37 dB and output 1-dB compression point of 14.5 dBm.

The measurements of the TX channel was performed in the same setup with

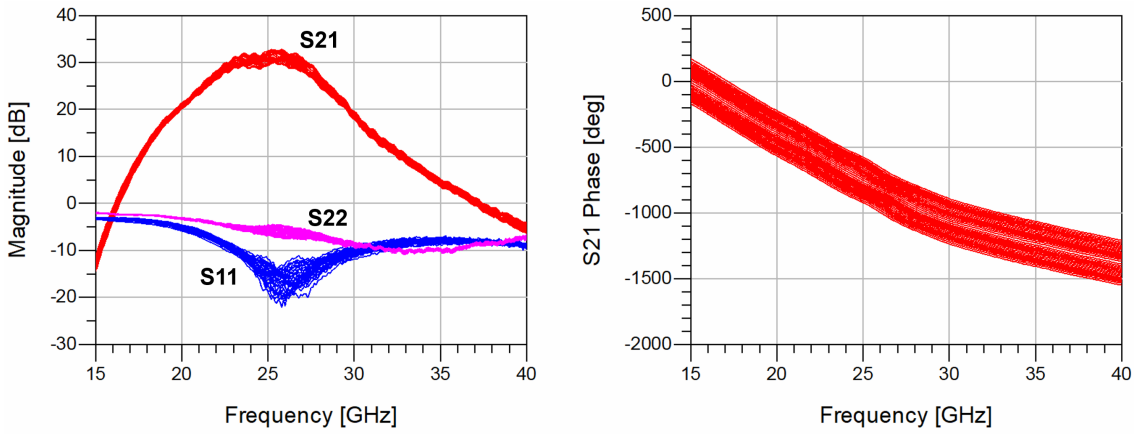


Figure 4.17: Measured S-parameters of the single TX channel for different phase settings. 32 major states are shown.

the RX channel (Fig. 3.16 and 3.17). The measured S-parameters are shown in Fig. 4.17. The TX channel achieves more than 30 dB average gain, with its input matching being better than 10 dB in between 23 and 29 GHz. Since the output of the PA is matched for maximum power, rather than maximum power transfer, the output return loss is around 5 dB. A smooth phase vs. frequency behavior was observed. Although there is a relatively large discrepancy between the simulate and measured gain levels, its behavior versus frequency is in agreement with simulations.

However, despite the fact that the measured small-signal performance as well as the dc operating points are in agreement with the designed and simulated values, some issues have been found in the large signal behavior of the TX channel. First, output 1-dB compression point is much lower than expected at only +3 dBm. This was measured again using the dc probes to provide the supply voltages. Second, in another effort (by Aselsan, REHIS) to characterize the TX channel, the die was wirebonded to an alumina laminate and placed inside a module as seen in Fig. 4.18. In that case, an oscillation was observed at the output of the TX channel at 25.88 GHz. It was found that the oscillation disappears once the bias voltages of the PA 2-nd stage is reduced below 1.2 V. However, despite our extensive efforts to back-track the problem, we were not able to regenerate this oscillation problem neither in our measurement setups at the university, nor in our simulation setups.

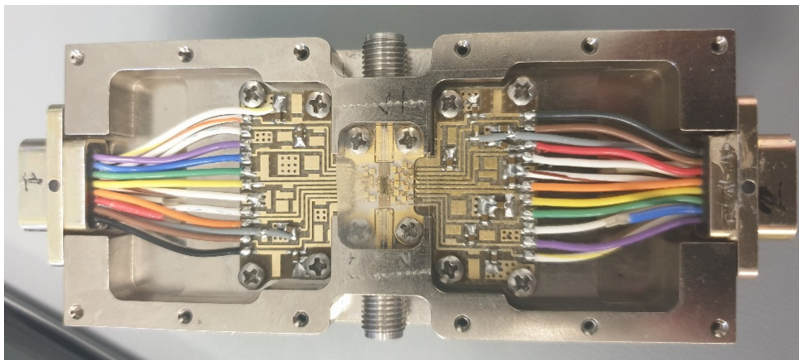


Figure 4.18: Single channel TX die mounted on an alumina substrate and placed within a mechanical module.

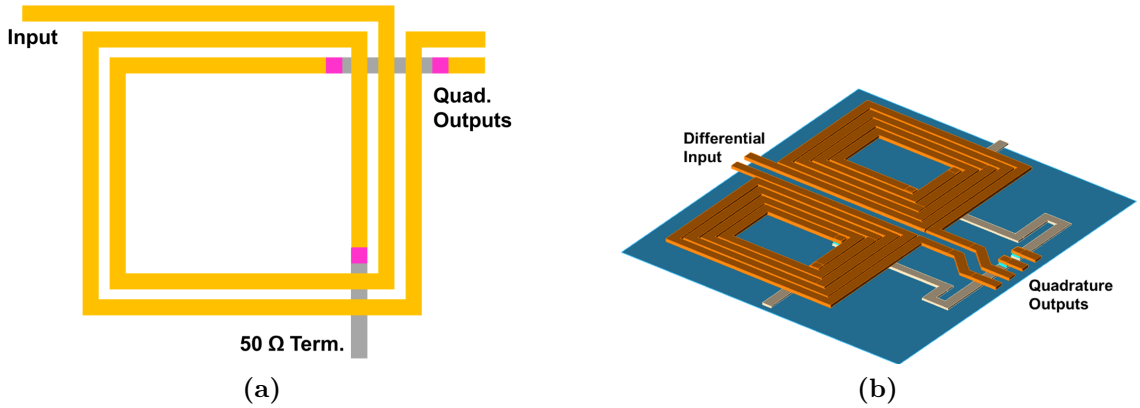
4.2 Four-Element Beamforming ICs

A number of modifications are made over the single-channel versions of both RX and TX beamformer channels.

- The simulated gains single RX and TX channels were higher than 30 dB. Although acceptable for massive-MIMO based operation, such high gain levels may become problematic when many such channels are combined on the same die for phased-array applications. It may cause oscillations due to unwanted (and hard to simulate) coupling effects between adjacent channels. Therefore, the TX channel gain is decreased by reducing the number of stages in the PA from two to one, and both RX and TX channel gains are further decreased using digitally controlled attenuators.

- The amplitude control specification of the four-element beamformer chips is set to 4-b control with 1-dB steps. The previously designed single-stage cascode VGA operates around 10-dB gain control range. If the gain control range is increased beyond this limit, the VGA exhibits strong phase variation across its gain settings, which is undesirable. Therefore, we decided to keep the VGA operating at 8-dB gain control with 1-dB steps, and utilize a 3-b digitally controlled step-attenuator with 1-dB steps, effectively reaching 4-b amplitude control.

- Finally, the height of the single beamformer channels was 0.62 mm, which was limited by the quadrature generation network, as can be seen from Fig. 4.10



(a) (b)

Figure 4.19: (a) Conventional on-chip coupled-line coupler designs (single-ended version). (b) Proposed miniaturized coupled-line coupler design (pseudo-differential version).

and 4.16. When used in a four-element array, this significantly increases the area and cost. Therefore, additional IQ generation schemes are investigated once again, and using a novel miniaturized coupled-line coupler the height of the channel is reduced to 0.4 mm.

4.2.1 Design Considerations and Updates

The previous LNA design was highly linear (OP1dB of 8 dBm), but the linearity of the RX channel was limited by the following blocks. Therefore, we relaxed the linearity (and hence the power dissipation) of the LNA, and its design is updated by my colleague Abdurrahman Burak. The updated LNA has a simulated gain of 15 dB, noise figure of 2 dB, OP1dB of 0 dBm (down from 8 dBm), and power consumption of 9 mW (down from 30 mW).

The PA was reduced to a single stage, by my colleague Alper Guner, without sacrificing its output power requirement. The updated single-stage PA has a gain of 13.5 dB, OP1dB of 15.5 dBm, and a dc power consumption of 50 mW.

The previous IQ generator for single-channels was based on lumped-element hybrid coupler, and its height (0.62 mm) was the limiting factor of the channel height. The updated IQ generator is shown in Fig. 4.19. It is based on a novel miniaturized coupled-line coupler. Regular coupled-line couplers employ two side-by-side transmission lines of length $\lambda/4$ with a gap in between such that half of the

input power couples to the other transmission line. Besides the fact that straight $\lambda/4$ lines at 26 GHz would occupy unfeasibly large chip area, it is impossible to place on-chip straight transmission lines close enough to achieve 3-dB coupling, due to design-rule-check (DRC) violations. Therefore, on-chip coupled-line couplers use the configuration shown in Fig. 4.19(a). The two transmission lines are intertwined around each other so that along the two edges of the rectangular shape, a line is coupled from both sides. This increases the coupling between the lines so that 3-dB coupling is possible, and at the same time reduces the area.

In this work, we even further miniaturized the structure, by doubling the number of turns from one to two, as shown in Fig. 4.19(b). In this novel IQ generator, coupling value is increased so that it is easier to achieve 3-dB coupling, and the IQ generator chip area (especially the height compared to the previous design) is greatly reduced. The total IQ generator area is 0.35×0.45 mm^2. It has an EM simulated insertion loss of 3.8 dB. The rest of the phase shifter design is the same as before.

Previously designed VGA for single-channels had an analog control voltage, and when it was swept with linear steps, the VGA exhibited almost linear-in-dB gain control. However, it is undesirable to have analog control voltages in an array and digital controls are preferred. For this reason, a 3-b current steering DAC was designed and integrated into the VGA, to achieve gain control with 1-dB steps. Also its layout was optimized by changing the shape of the base inductor and number of turns of the collector inductor to make it more compact. The final layout of the VGA is shown in Fig. 4.5(b), occupying an area of only 0.3×0.3 mm^2. The VGA has an EM-simulated gain in the range of 6-13 dB, noise figure between 3-5 dB, rms amplitude error of 0.2 dB, and phase variation of $\pm5^\circ$ across its different gain settings. Its output P1dB is 6 dBm, the RF core consumes 12 mA from a 2.5 V supply, and the DAC draws 2.5 mA from a 3 V supply, for a total dc power consumption of 36 mW.

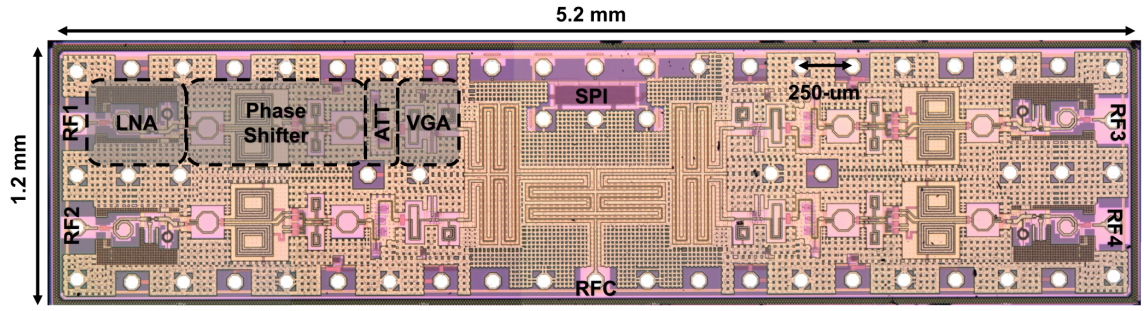


Figure 4.20: Die photo of the four-channel analog beamforming receiver IC. Die size is 6.25 mm^2.

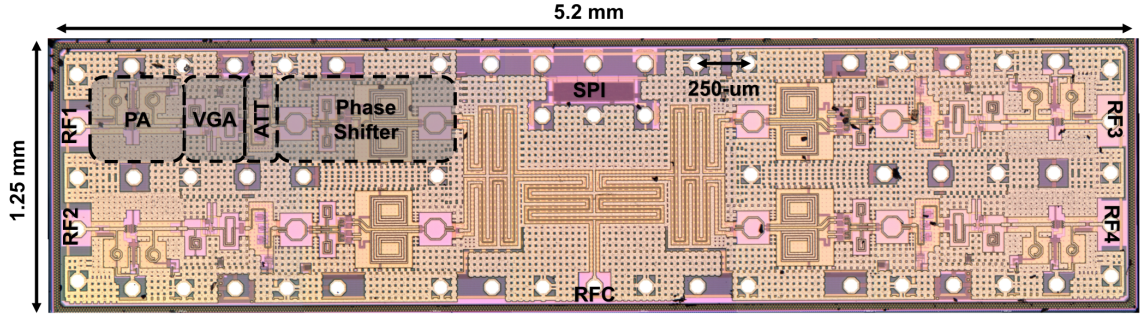


Figure 4.21: Die photo of the four-channel analog beamforming transmitter IC. Die size is 6.5 mm^2.

4.2.2 Simulation Results

The four-channel RX and TX beamformer ICs were fabricated in IHP sG13S SiGe BiCMOS process. The can be seen in Fig. 4.20 and Fig. 4.21. These ICs were designed specifically for flip-chip packaging. Progress has been made on that front, as will be discussed in the next section. Here, the simulation results will be shared.

Fig. 4.22-4.24 summarize the EM simulated performance of the four-element RX beamformer. The single RX channel has an average gain of 18 dB from the LNA input to the combiner output. So, this value includes the systemic Wilkinson combiner loss of 3 dB and the ohmic losses in the combiner. When all the channels will be used in the array, the total electronic gain will be $18 + 10 \log 4 = 24$ dB. The total receiver noise figure is 3.5 dB, and the input-referred 1-dB compression point is -25 dBm. The dc power consumption per channel is $9 + 11 + 30 = 50$ mW, and the total dc power consumption of the RX beamformer is 200 mW. Its input/output is well matched at 26 GH center frequency.

Fig. 4.25-4.26 summarize the EM simulated performance of the four-element

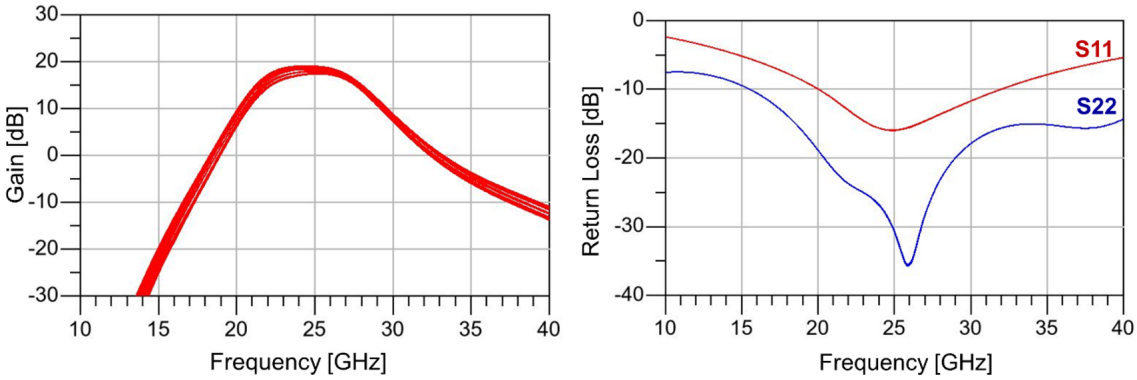


Figure 4.22: Simulated (a) gain and (b) input/output return loss across different phase settings.

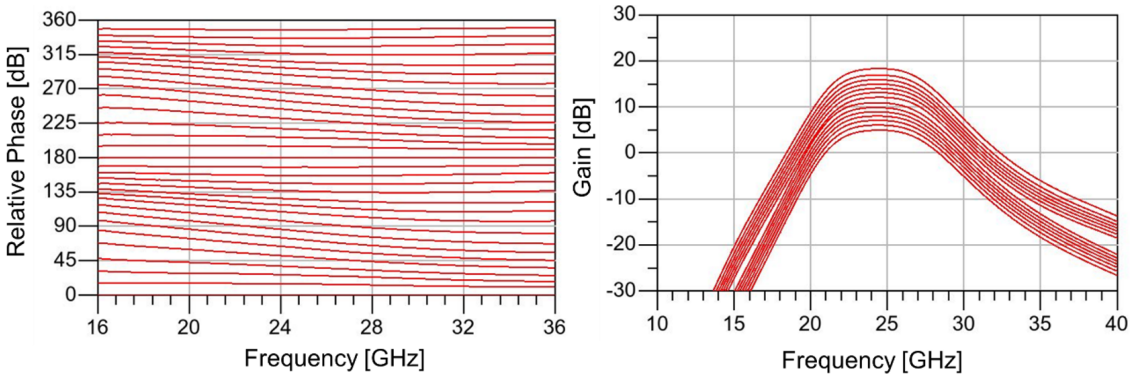


Figure 4.23: (a) Simulated relative insertion phase across different phase settings and (b) simulated 4-b amplitude control functionality.

TX beamformer. It has an average 17 dB gain from the Wilkinson divider input to the PA output, taking into account the systemic and ohmic losses of the Wilkinson. The output 1-dB compression point of a single TX channel is 12.5 dBm. The power dissipation per TX channel is $36 + 11 + 50 = 97$ mW and the total dc power consumption is 388 mW.

4.2.3 Flip-Chip Packaging and Measurement Considerations

The four element beamformer ICs were designed specifically for flip-chip packaging. Typical pad-to-pad pitch size for flip-chip packaging with C4 bumps is about 400-μm. However, in this work we were limited by the fact that two RF input/ouptuts must be placed on the right/left edges of the die. This limits the maximum pad pitch size to 250-μm since a GSGSG interface is necessary to satisfy impedance

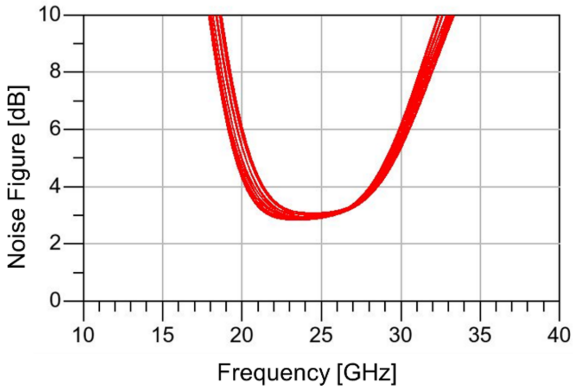


Figure 4.24: Simulated NF of the RX channel across different phase settings.

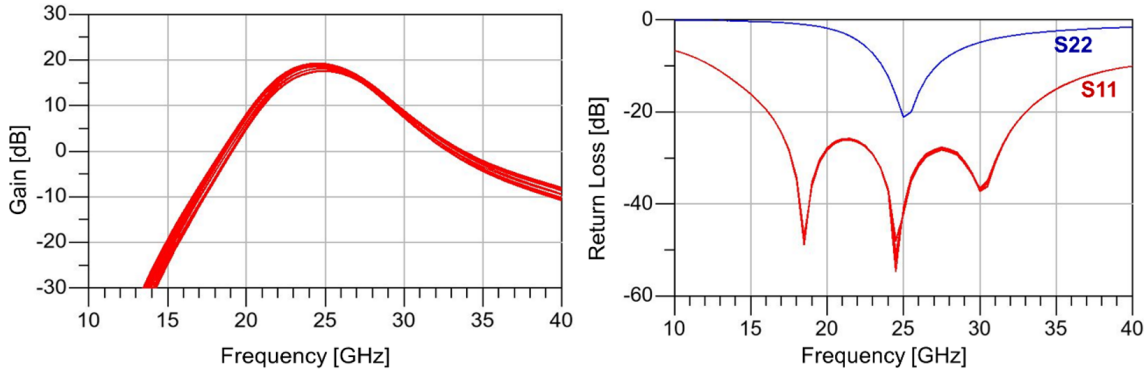


Figure 4.25: Simulated (a) gain and (b) input/output return loss across different phase settings

matching and port-to-port isolation at 26 GHz. Although possible, using C4 bumps in such a small pitch size is not reliable. Hence, alternative bumping techniques were considered such as, copper pillar and gold stud bumping. The former mostly requires wafer level processing and was not suitable for our beamformer dies. So, even though it is much more costly, gold stud bumping is chosen in this work. Since gold does not disperse as much as solder when heated, the smaller pad pitch size is not a concern. A single stud height is on the order of 30-μm and it is possible to stack two studs on top of each other to achieve 60-μm total height. The latter option is preferred in terms of RF performance, since the shunt capacitance to the pcb ground plane under the IC will be minimized.

Another challenge in flip-chip packaging for this work stems from the fact that lots of dc supply/bias/control voltages are required. Some of the pads for supply voltages could have been combined together, but it was not preferred for debugging purposes. Due to the large number of supply/bias/control pads, a four-layer pcb

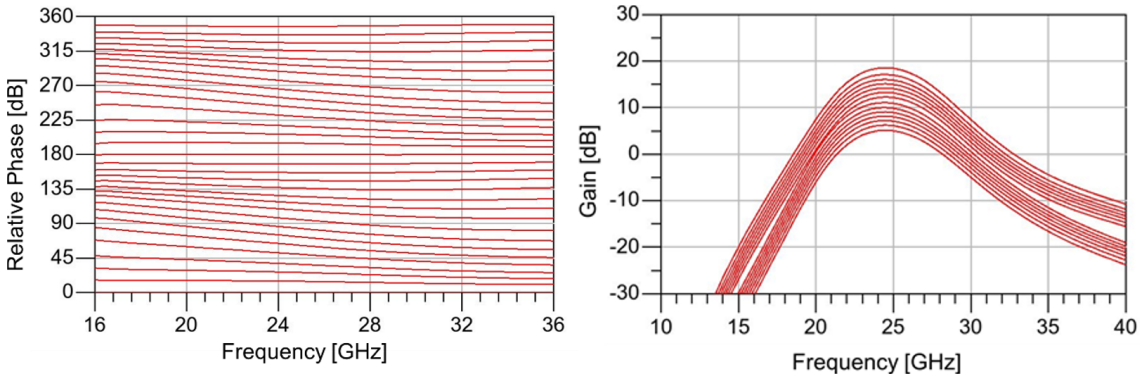


Figure 4.26: (a) Simulated relative insertion phase across different phase settings and (b) simulated 4-b amplitude control functionality.

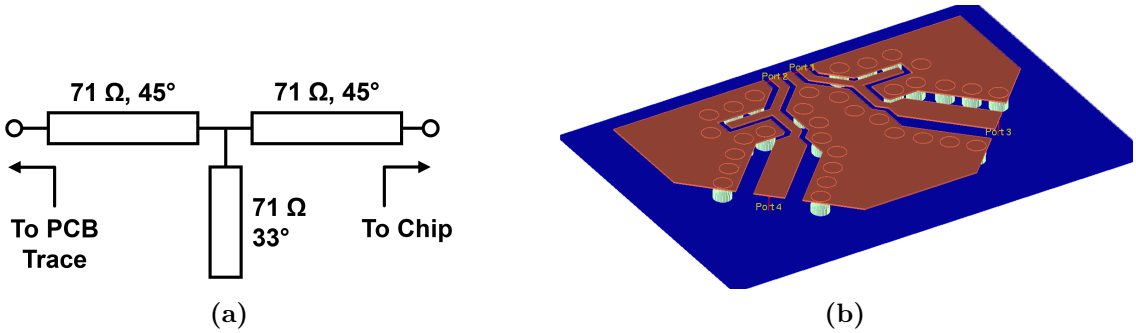


Figure 4.27: (a) Schematic view of the chip-to-pcb transition using high impedance transmission lines. (b) 3D em view of the transition.

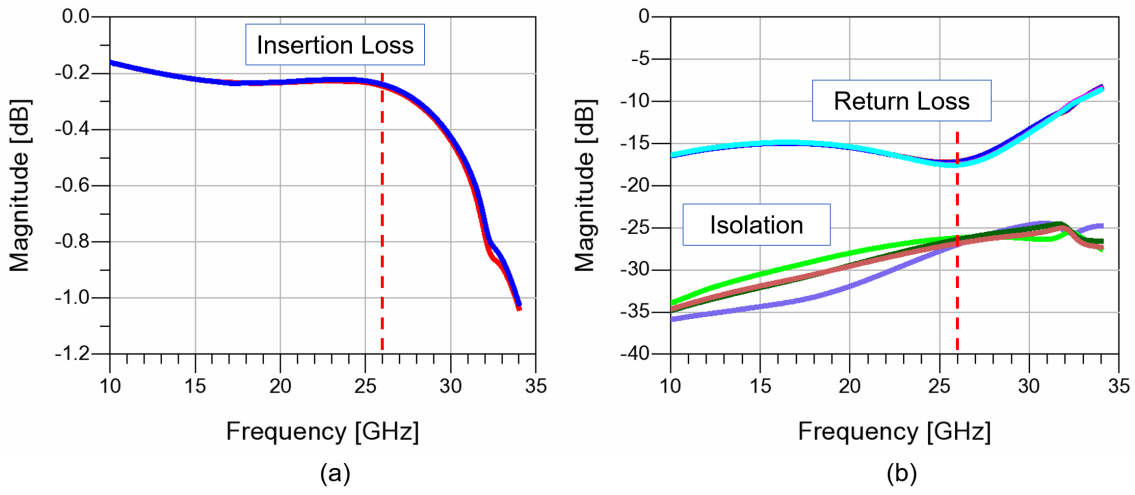


Figure 4.28: Simulated (a) insertion loss, (b) return loss and isolation of the chip-to-pcb transition.

stack is necessary. The layers are ordered from top to bottom as RF / GND / Power / GND. The top layer is 10 mil RO4350B, which has a dielectric constant of 3.66 and a tangent loss of 0.003 at 2.5 GHz. The total height of the pcb stack is 1 mm.

The geometry of the pcb traces right next to the four RF interfaces are limited

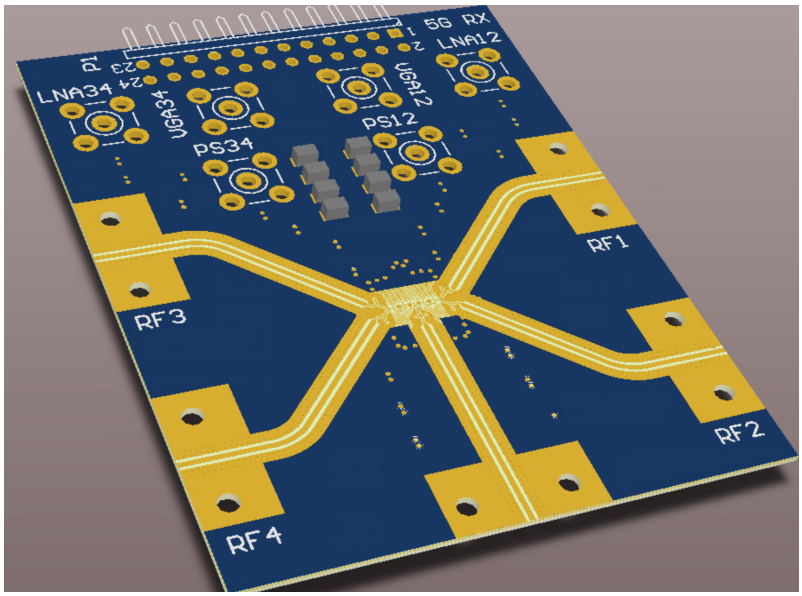


Figure 4.29: Final layout of the 4-stack RF pcb for direct flip-chip packaging of the beamformer dies.

by the pad pitch size of 250-μm. A 50-Ω CPWG transmission line requires a trace width of 0.5 mm and a ground plane gap of 0.3 mm. Therefore, in this pcb stackup, it is not possible to create a 50-Ω transmission line right next to the bumps of the IC. Therefore, a matching circuit is needed for the transition from IC to the 50-Ω line. This is achieved with an open stub-matching using higher impedance transmission lines, as seen in Fig. 4.27(a). All the lines have a 71 Ω characteristic impedance, which is the lowest value that can be achieved right next to the IC. This transition is 3D EM simulated in ADS, as can be seen in Fig. 4.27(b). The results are shown in Fig. 4.28. Insertion loss is better than 0.25 dB up to 26 GHz and better than 0.3 dB up to 28 GHz. Up 29 GHz, return losses of all four ports are better than 15 dB and port-to-port isolations are better than 25 dB. At 28 GHz, half of the total loss of 0.3 dB comes from imperfect matching (15 dB return loss) and the other half comes from the dielectric losses. This number is inline with the simulated line loss of the pcb stackup, which is about 0.25 dB/cm. The layout of the final pcb design is shown in Fig. 4.29.

This section presented design and measurement of RX and TX single-channel beamforming ICs in 130-nm SiGe BiCMOS. Better than state-of-the-art noise figure performance was obtained in the single RX channel, both ICs achieved around 30 dB

gain, and they feature 6-b phase and 3-b amplitude control capability. Additionally, the development of four-element phased-array beamforming ICs was discussed and the most recent simulation results are presented.

Chapter 5

Conclusion and Future Work

5.1 Summary of Work

Next generation (5G) mobile communication systems require extremely high data rates, higher spectral efficiency, extremeley low latencies, and better cost efficiency. These challenging specifications necessitate the use of a combination of technologies that would have seemed not suitable for mobile cellular communications just a few years ago, such as mm-wave frequencies, phased-array transceivers, and full-duplex radios.

In this thesis, circuit and system level solutions, implemented in 130-nm SiGe BiCMOS, were presented targeting the above mentioned specifications of future 5G networks. More specifically, a full-duplex transceiver front-end was presented featuring an on-chip self-interference cancellation circuitry in the form a high-resolution I/Q vector modulator followed by switched-Π type attenuators and linear-in-dB controlled variable-gain amplifiers. The measured I/Q modulator achieved state-of-the-art performance with 10-b monotonic phase states, with a maximum phase deviation of 0.65° between any adjacent states.

To complement the full-duplex transceiver front-end, phased-array beamforming ICs are designed. Single-channel RX and TX beamformers were developed for massive-MIMO systems and four-element RX and TX beamformers were designed for phased-array operation. The single receiver channel achieved better than state-

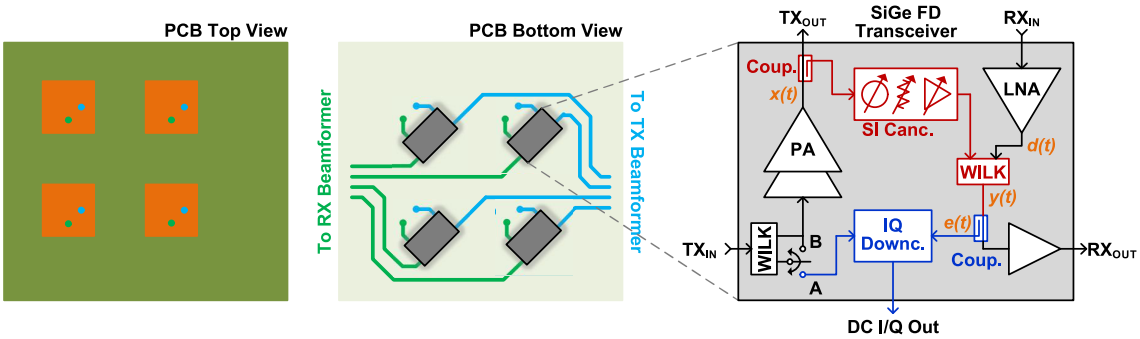


Figure 5.1: One possible way of combining the full-duplex SI cancelling transceiver with the four-element RF phased-array beamformering ICs.

of-the-art performance with 3.3 dB NF and 28.5 dB gain.

5.2 Future Work

In the short term, both the four element beamforming ICs and the full-duplex transceiver front-end will be subject to further characterization and measurements. There has been ongoing efforts on flip-chip packaging of the four-element beamformer ICs. After their completion, performance of the ICs will be measured using end-launch SMA connectors. Furthermore, we experienced some unexpected delays regarding the fabrication of the low-power IQ downconverter chip and the complete full-duplex transceiver chip, caused by the foundry itself (IHP Microelectronics). Once those dies were fabricated and shipped, their performance will be measured with the RF probe station setup.

There are several aspects both in the full-duplex transceiver and the four-element beamformers that can be improved in the next iterations. For instance, a much better SPI interface that allows powering down a specific beamforming channel would be very useful. Furthermore, reducing the number of dc/control pads of both ICs would significantly ease the testing procedures.

As a long term future work, it may be possible to combine the functionalities of both ICs either on the same die, or in a system as shown in Fig. 5.1. Today, vast challenges lie ahead of the concept of full-duplex beamforming phased-arrays, but someday it will be a reality.

Appendix A

IHP 130-nm SiGe BiCMOS (SG13S) Process

This process offers HBTs with a reported f_T/f_{max} of 250/340 GHz, CE breakdown voltage of 1.7 V, 5 thin and 2 thick top metal layers (6th metal is 2-μm and 7th metal is 3-μm thick), 1.2 V logic and 3.3 V I/O CMOS, poly resistors with 250 and 1300 Ω/sq, and MIM capacitors with 1.5 fF/μm^2 density.

Fig. A.1 shows the simulated f_T, f_{max}, and NF_{min} of the process for an HBT of size $8 \times 0.48\mu m \times 0.12\mu m$. Both f_T and f_{max} peaks around 10 mA of collector current for the specified device dimensions, with NF_{min} bottom peak occurring, expectedly, at much lower current levels of 1–3 mA. However, it must be noted that these results represent the transistor-only performance, and they degrade if the connections of transistor terminals to the top metal is included.

Finally, Fig. A.2 shows a list of single-ended and differential transmission lines with different geometries, which were used throughout all the work reported in this dissertation.

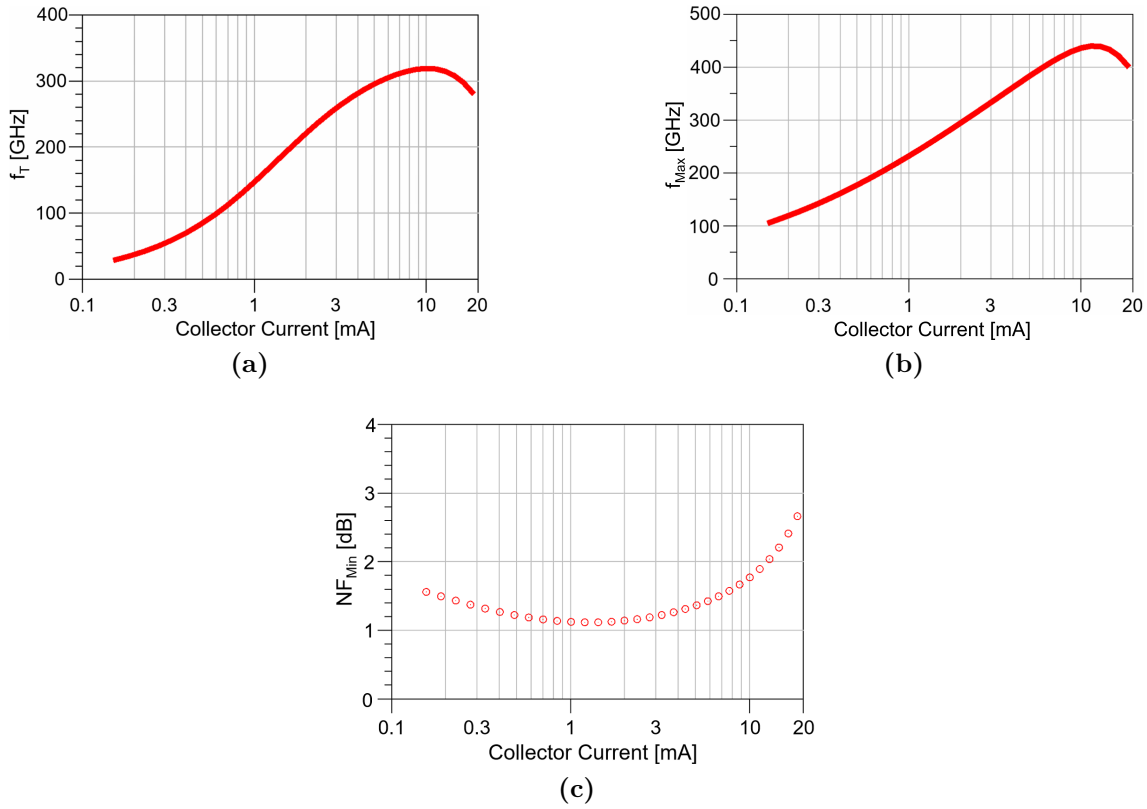


Figure A.1: Simulated (a) f_{T}, f_{Max} and $\mathrm{NF}_{\mathrm{Min}}$ of HBTs in IHP SG13S technology.

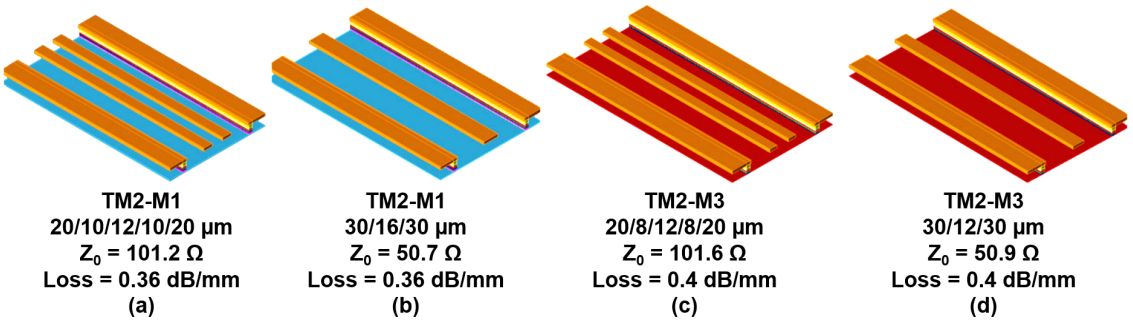


Figure A.2: Single-ended and differential grounded coplanar waveguideeeee (GCPW) transmission lines designed in IHP SG13S technology.

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